QUESTION PAPER

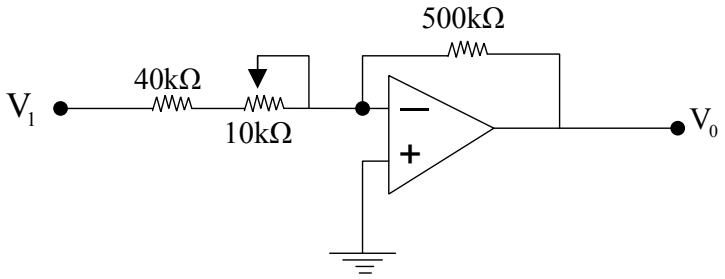
Name: **Enrolment No:**	UPES

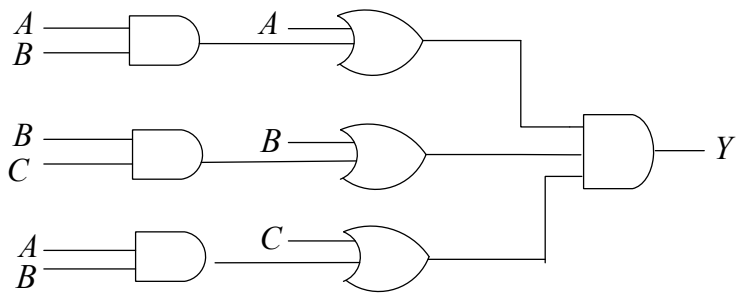
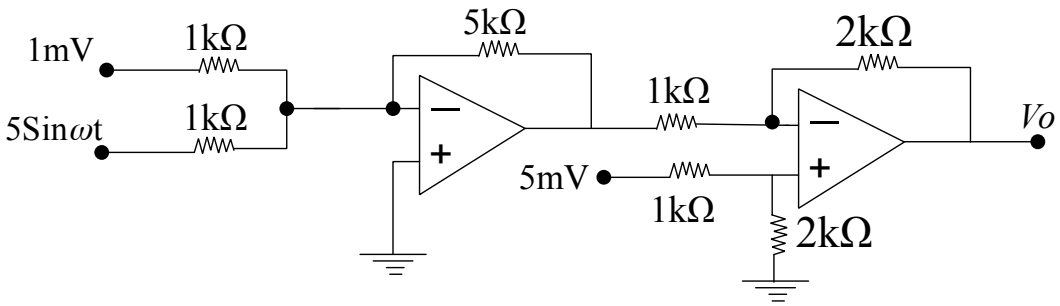
UNIVERSITY OF PETROLEUM AND ENERGY STUDIES
End Semester Examination, December 2018

Course: Analog and Digital Electronics (ECEG-2002) **Semester: III**
Program: B. Tech- Mechatronics
Time: 03 hrs. **Max. Marks: 100**

Instructions: Attempt all the sections.

SECTION A (20 Marks)

S. No.	**Answer all the questions.**	**Marks**	**CO**
Q 1	Draw the circuit diagram of a single stage transistor amplifier, state the function of each component used in this circuit.	**4**	**CO1**
Q 2	The voltage gain of an amplifier without feedback is 1000. It decreases to 100 with feedback. Evaluate the feedback factor.	**4**	**CO1**
Q 3	Evaluate the range of the voltage gain adjustment in the circuit shown in Fig. (1) as,  **Fig. (1)**	**4**	**CO2**
Q 4	Write the Boolean expression for the logic diagram given below and simplify it as much as possible.	**4**	**CO3**

	 **Fig. (2)**		
Q 5	Sketch the block diagram of the combinational and sequential logic circuits. How both are differing on the basis of memory element and time dependent operation.	**4**	**CO4**
	SECTION B (40 Marks)		
	Answer all the questions.		
Q 6	Design a logic gate diagram of the obtained minimize expression using Universal 'NOR' gate. The Boolean expression is: $Y = A + B\left(AC + \left(B + \overline{C} \right) D \right)$	**10**	**CO3**
Q 7	Determine the output voltage of the circuit shown in Fig. (3).  **Fig.(3)**	**10**	**CO2**
Q 8	Find the minimal sum of product for the Boolean expression F= ∑m (1, 2, 3, 7, 8, 9, 10, 11, 14, 15) using Quine- McCluskey method.	**10**	**CO3**
Q 9	**Attempt both the parts:** **(a)** Elucidate the data transmission operation in the shift registers. **(b)** Design and analyze the operation of a 4-bit serial in- serial out shift register.	**10**	**CO4**
	SECTION-C (40 Marks)		
	Answer all the questions.		
Q 10	Design the combinational logic circuit for (i) an Even Parity Bit Generator for a 4-bit (A, B, C, D) input data (ii) an Odd Parity Bit Generator for a 4-bit (A, B, C, D) input data	**10+10**	**CO3**

Q 11	• **Attempt both the parts:** **(a)** Design a combinational logic circuit diagram that accepts a 4-bit Gray code (G4, G3, G2, G1) and provide 4-bit binary code (B4, B3, B2, B1). **(b)** Design and analyze the operation of a synchronous mode-6 Gray code converter using 'T' Flip-flop. **OR** Implement the following function using 8:1 MUX- $F(x,y,z) = \sum m\ (0, 2, 3, 5)$	**10+10**	**CO3/ CO4**

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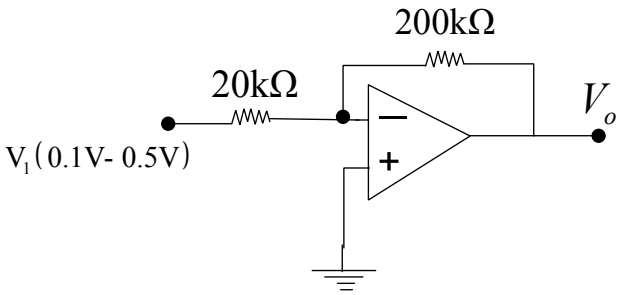
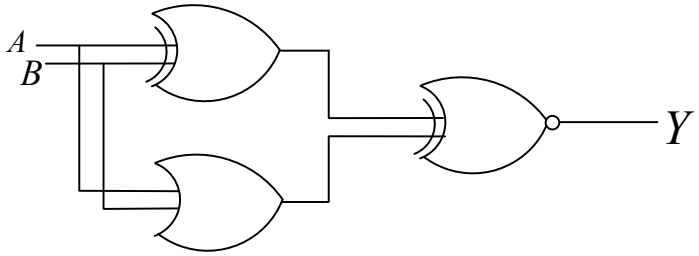
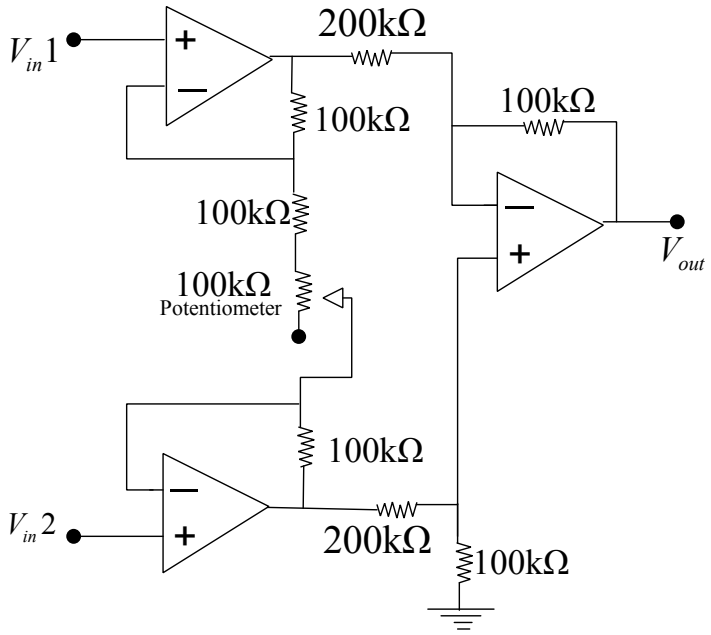
SECTION A (20 Marks)

S. No.	**Answer all the questions.**	**Marks**	**CO**
Q 1	Given $h_{ie} = 2.4k\Omega$, $h_{fe} = 100$, $h_{re} = 4 \times 10^{-4}$ and $h_{oe} = 25\mu S$. Sketch the common emitter hybrid equivalent model.	**4**	**CO1**
Q 2	A single stage transistor amplifier has a voltage gain of 600 without feedback and 50 with feedback. Find the percentage of output which is feedback to the input side.	**4**	**CO2**
Q 3	What is the range of the output voltage in the circuit of Fig. (1). If the input voltage can vary from 0.1V to 0.5V ?  **Fig. (1)**	**4**	**CO3**

Q 4	Redraw the circuit given in Fig. (2) after simplification  **Fig. (2)**	**4**	**CO3**
Q 5	**Attempt all the parts:** (i) $(158)_{BCD} \rightarrow (?)_2 \rightarrow (?)_{10}$ (ii) $(1246)_{10} \rightarrow (?)_{\text{Excess-3 code}}$ (iii) $(1011110)_2 \rightarrow (?)_{\text{Gray Code}}$	**4**	**CO4**
	SECTION B (40 Marks)		
	Answer all the questions.		
Q 6	Minimize the minterm using (i) SOP and (ii) POS expressing using K-map F(ABCD)= ∑m(2, 3, ,6, 7, 10, 11, 12)	**10**	**CO4**
Q 7	The circuit shown in Fig. (3) is an instrumentation amplifier. Determine the range which its gain can be varied if potentiometer is varied over its entire range.  **Fig. (3)**	**10**	**CO2**
Q 8	Draw the logic diagram using only two input NAND gates to implement the	**10**	**CO3**

	F= $\left(AB + \overline{A}\,\overline{B} \right)\left(C\,\overline{D} + \overline{C}\,D \right)$ following Boolean expression		
Q 9	Design and analyze the operation of parallel in- parallel out shift registor. **OR** Design and analyze the operation of 3-bit up counter, which has counting sequence 000, 001, 010, 011, 100, 101, 110, 111, 000, ……. Using J-K Flip-flops.	**10**	**CO4**
	SECTION-C (40 Marks)		
	Answer all the questions.		
Q 10	Design the logic diagram using NAND universal gate of obtained reduced expression of minimal expression for F= ∑m (6, 7, 8, 9) + d(10, 11, 12, 13, 14, 15) using Quine- McCluskey method.	**20**	**CO3**
Q 11	• **Attempt both the parts:** (a) Design a synchronous BCD counter using J-K Flip-flops. (b) Design a circuit that can be built using AOI logic and outputs a '1' when a 4-bit hexa-decimal input is an odd number from 0 to 9. **OR** Design a 5-bit comparator using a single 7485 4-bit comparator.	**10+10**	**CO4/ CO3**