Name: **Enrolment No:**	

UPES

End Semester Examination, December 2025

Course: Digital Electronics **Semester: I**

Program: BSc-CSE **Time: 03 hrs.**

Course Code: ECEG1010 **Max. Marks: 100**

Instructions: Please attempt according to the provided time and given weightage.

S. No.		Marks	CO
	SECTION A		
Q 1	Design Ex-OR & Ex-NOR Gate using NAND Gate.	**4**	**CO1**
Q 2	Design the truth table and draw the circuit diagram of a 3-bit Binary-to-Gray code converter.	**4**	**CO1**
Q 3	Simplify the function $F(A, B, C, D) = \Sigma m(1, 4, 6, 8, 9, 11, 13, 14,15)$ using a 4-variable K-map.	**4**	**CO2**
Q 4	Convert a D flip-flop into a T flip-flop.	**4**	**CO3**
Q 5	Differentiate in between Combinational and Sequential circuits.	**4**	**CO4**
	SECTION B		
Q 6	State and prove De Morgan's Theorem for 3 variables.	**10**	**CO1**
Q 7	Design and explain a full adder using a decoder circuit. **OR** Design a combinational circuit to detect whether a 4-bit binary number is divisible by 2 or not.	**10**	**CO2**
Q 8	Design and explain an S-R flip-flop.	**10**	**CO3**
Q 9	Design a MOD-16 asynchronous up-counter using negative-edge-triggered J-K flip-flops.	**10**	**CO4**
	SECTION-C		
Q 10	a) What is the Race-Around Problem? How can it be eliminated? b) Explain the working of a 4-bit magnitude comparator. Draw the logic diagram and write the expressions used to compare two binary numbers A and B.	**10** **10**	**CO3**
Q 11	a) Write a short note on Shift register along with its applications. b) Design a 4-bit synchronous up counter using T flip-flops. Show all the excitation tables and logic diagrams.	**10** **10**	**CO4**