Name:

Enrolment No:

UPES

End Semester Examination, Dec 2025

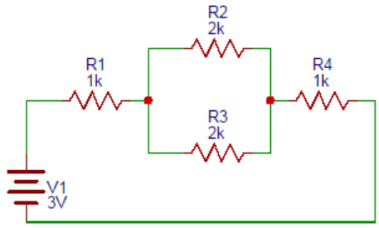
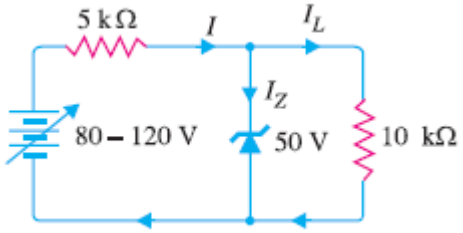
Course: Basic Electrical and Electronics Engineering **Semester: I**

Program: B. Tech- All SoAE Branches **Time : 03 hrs.**

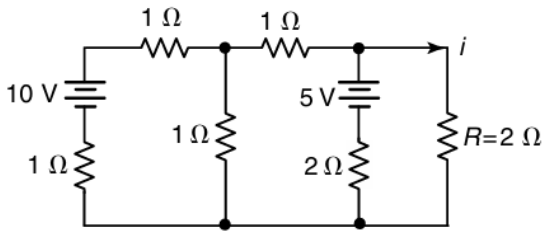
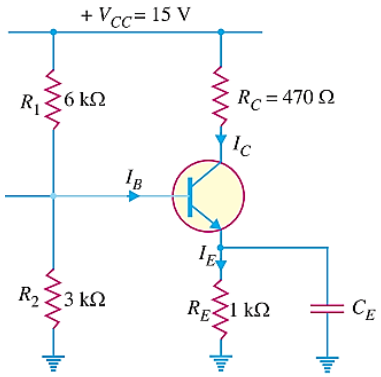
Course Code: ECEG-1013 **Max. Marks: 100**

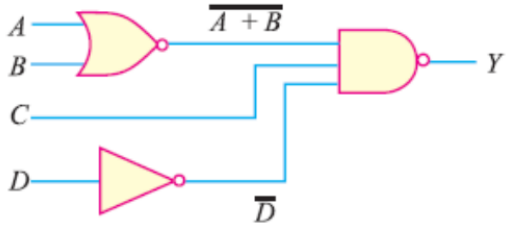
Instructions: Attempt all the sections.

SECTION A
(5Q×4M=20Marks)

S. No.	**Attempt all the questions.**	**Marks**	**COs**
Q 1	Determine the voltage drop across the Resistance R4 (1k ohm) in the circuit as shown in Fig. (1),  **Fig. (1)**	**4**	**CO1**
Q2	Find the maximum and minimum values of zener diode current.  	**4**	**CO1**
Q3	Define the following: (i) Operating point-Q (ii) DC load line (iii) current gain for CE configuration in Bipolar junction transistor (BJT).	**4**	**CO2**
Q4	Convert the following: (a) $(100101011)_2 = (\ ?\ )_4$ (b) $(305.B2)_{16} = (\ ?\ )_8$ (c) $(1110101)_{Gray\ code} = (\ ?\ )_{Binay\ code} = (\ ?\ )_{10}$	**4**	**CO2**
Q5	Brief the principle of electromechanical energy conversion. Give appropriate examples of machines that transfer electrical energy to mechanical energy and vice versa.	**4**	**CO1**

SECTION B
(4Q×10M= 40 Marks)

Q 6	A manufacturing plant uses a digital Safety Control Module that continuously monitors four critical inputs: • **A** – Machine Mode (0 = Production Mode, 1 = Maintenance Mode) • **B** – Safety Gate Status (0 = Open, 1 = Closed) • **C** – Temperature Alarm (0 = Normal, 1 = Overheat) • **D** – Hydraulic Pressure Alarm (0 = Normal, 1 = High) The system must generate a STOP signal F when dangerous or abnormal operating conditions occur. Based on engineering analysis, the STOP signal should turn **ON** for the following operating combinations, represented by the minterms: **F(A, B, C, D) = ∑ m(2,3,6,7,8,10,13,15)** **Using the above real-world safety scenario:** a) Minimize the STOP-signal function F(A, B, C, D) using a 4-variable Karnaugh map (K-map)**.** b) Draw the logic circuit diagram corresponding to the minimized Boolean expression.	**10**	**CO3**
Q7	Draw the Thevenin's equivalent of the circuit in Figure (2) and find the load current, *i*.  Fig. (2)	**10**	**CO2**
Q8	Figure (3) shows the voltage divider/self-biasing circuit. Draw the DC load line and determine the operating point (Q).Assume the transistor to be silicon. Also the current amplification factor for common emitter is given 100.  Fig. (3)	**10**	**CO3**
Q9	The four diodes used in a bridge rectifier circuit have forward resistances which may be considered constant at 1Ω and infinite reverse resistance. The	**10**	**CO3**

	alternating supply voltage is 240 $V_{r.m.s.}$ and load resistance is 480 Ω. **Calculate** (i) maximum load current (ii) output DC load current (iii) maximum AC voltage (iv) output DC voltage and (v) power dissipated in each diode. Also design the bridge full wave rectifier circuit.		
SECTION-C (2Q×20M=40 Marks)			
Q 10	**Attempt both the parts** **(a)** A single phase 3300/240 V, 50 Hz transformer has a maximum magnetic flux of 0.0315 Wb in the core. Calculate the number of turns in primary and secondary windings. **(b)** A DC generator has an armature e.m.f of 100V when the useful flux per pole is 20mWb and the speed is 800 rpm. Calculate the generated e.m.f. • with the same flux and a speed of 1000 r.p.m. • with a flux per pole of 24mWb and speed of 900 r.p.m.	**10+10**	**CO4**
Q11	**Attempt both the parts:** (a) Minimize the following terms using K- map $f(A,B,C,D) = \sum m\ (0, 1, 2, 3, 5, 7, 8, 9, 10, 12, 13) + d(4,9)$ (b) Using Boolean techniques, simplify the following expression. Also realize the minimized expression using NOR gate. Y= AB+A(B+C)+ B(B+C) **OR** **Attempt both the parts:** **(a)** Map the following POS function using K-map and implement the minimized expression using logic gates: $f = (A + B + C)(\overline{A} + B + \overline{C})(\overline{A} + \overline{B} + \overline{C})(A + \overline{B} + \overline{C})(\overline{A} + \overline{B} + C)$ **(b)** Determine the output Boolean expression for the given logic gate circuit shown in Figure (4). Also implement the obtained expression using (a) NAND (b) NOR logic gates.  **Fig. (4)**	**10+10**	**CO3**