Name: **Enrolment No:**	

UPES

End Semester Examination, May 2023

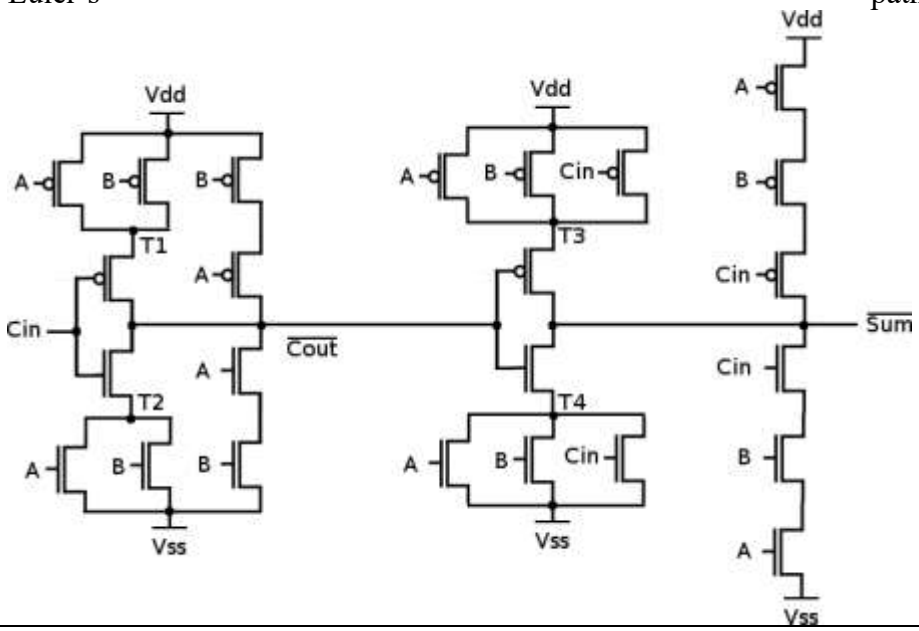
Course: VLSI Design **Semester: VI**

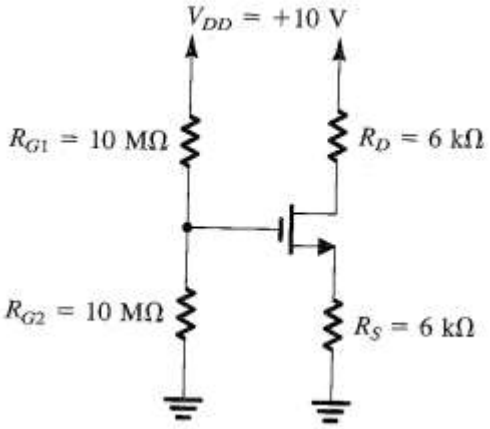
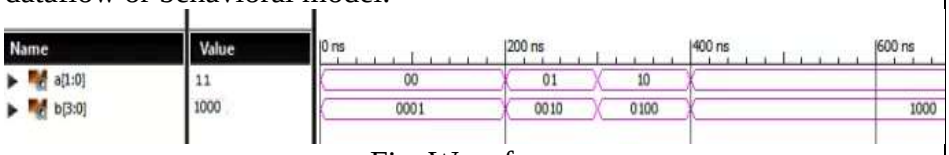
Program: B.Tech Electronics & Communication Engineering **Time : 03 hrs.**

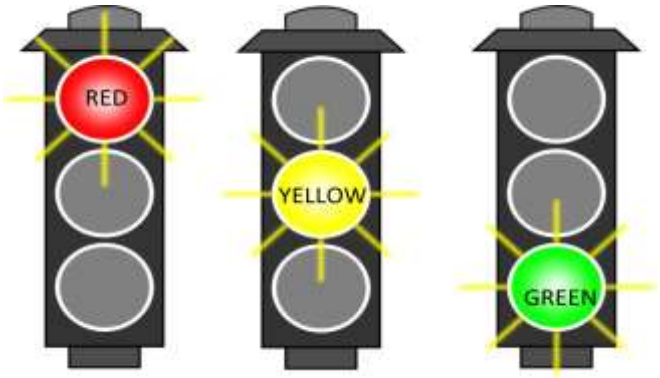
Course Code: ECEG-3049 **Max. Marks: 100**

SECTION A

(5Q x 4M = 20Marks)

S. No.		Marks	CO
Q 1	What is ASIC ? List the different abstraction levele of ICs and suggest the suitable examples.	**4M**	**CO1**
Q 2	Explain the Noise Margin and speed of operation of digital circuits. A logic gate is defined by the following volatge levels $V_{OH} = 5\ V$ $V_{OL} = 0.2\ V$ $V_{IH} = 2.5\ V$ $V_{IL} = 0.8\ V$ Find the noise margin of this gate.	**4M**	**CO2**
Q 3	Justify the output of the following logic diagram and show the minimum Euler's path. 	**4M**	**CO3**
Q 4	Design the decoder chip (3 x 8) using VHDL	**4M**	**CO5**

Q 5	Draw the large signal model of NMOS and PMOS with the complete description	**4M**	**CO1**
	SECTION B **(4Qx10M= 40 Marks)**		
Q 6	Explain the working of enhancement type NMOS and detail V-I characteristics in all regions. Derive the mathematical expression for the drain current in all the regions.	**10M**	**CO2**
Q 7	Draw the stick diagram and layout for CMOS inverter, 2 input XOR and 2 input NOR logic, Mark the all layers with exact colour and discuss the functionality to support your answer.	**10M**	**CO4**
Q 8	Derive the mathematical expressions to estimate the value of V_{OH}, V_{OL}, V_{IL} and V_{IH} for NMOS inverter circuit and detail the functionality with voltage transfer characteristics with resistive load. ***OR*** Analyze the circuit shown in Fig. to determine the voltage at all the nodes and the current through all the branches, Let V_t =1 V, $K_n'(W/L)$ =1 mA/V^2, and neglect the channel length modulation, $\lambda = 0$ 	**10M**	**CO3**
Q 9	**(a)** Design the CMOS logic Implementation for the followings $Y = \overline{A[B + C(D + E)]}$ $Y = \overline{A(B + CD) + E}$ Calculate the W/L ratio of the transistors involved in the design. **(b)** Identify the waveform shown in Fig. and draw the logic diagram and truth table for the same chip. Develop the VHDL code for the IC using dataflow or behavioral model.  Fig. Waveform	**10M** **(5+5)**	**CO4**

	SECTION-C **(2Qx20M=40 Marks)**		
Q 10	Compare the Melay and Moore FSM with examples. In the Case study "Traffic Light Control", the fundamental idea is to control the traffic. It can be used to avoid the vehicular collisions and traffic jams. This project is just a one-way traffic controller, although it can be further modified as well. Project will work in a way, it provides the instruction to the driver whether to drive through the intersection or yield at the intersection. ***Control Lights Indication*:** There are three control lights or signals, which will provide the instruction to the driver. **RED Light** – instructs the driver to STOP at the intersection. **YELLOW Light** – instructs the driver to WAIT (If red light is next) or GET READY (if green light is next) **GREEN Light** – instructs the driver to GO through the intersection.  Fig. Traffic Light Controller Fig. 2 presents the conditions of traffic light controller. Develop the HDL code to control the traffic intensity from one side. Also draw the state diagram show the test cases to test the design **OR** Design the Hardware Chip for the following using VHDL and draw the logic diagram for the same. **(a)** Full adder **(b)** Full Substractor **(c)** Encoder (8x3) **(d)** Odd Parity Generator and Checker (9-bit)	**20M**	**CO4**
Q 11	Draw the cross section view of CMOS under fabrication process. List the all steps required to fabricate the CMOS chip using N-well and P-Well process. Detail the complete operations required to fabricate the same chip.	**20M**	**CO2**