Name: **Enrolment No:**	

UNIVERSITY OF PETROLEUM AND ENERGY STUDIES
End Semester Examination, May 2023

Course: **Digital Electronics** **Semester:** **IV**
Program: **B. Tech- Renewable & Sustainable Engineering** **Time** **: 03 hrs.**
Course Code: **ECEG-2016** **Max. Marks: 100**

Instructions: Attempt all the sections.

SECTION A
(5Qx4M=20Marks)

S. No.	**Attempt all the questions.**	**Marks**	**CO**
Q 1	Simplify the following Y= $(A+B)\overline{AB}$ and construct the logic diagrams using NAND gates.	**4**	**CO1**
Q2	Reduce the following function using K-map and identify the prime implicants and non- prime implicants in Product of Sum (POS) form. $f = \sum m(2,3,6,7,10,11,12)$	**4**	**CO2**
Q3	How combinational circuit and sequential logic circuit is different from each other? What are the real-world applications and necessity in human life of both type circuits?	**4**	**CO3**
Q4	Determine the resolution of (a) a 6-bit DAC and that of (b) a 12-bit DAC in terms of percentage.	**4**	**CO4**
Q5	A certain memory has a capacity of 8K×16. (a) How many data input and data output lines does it have? (b) How many address lines does it have?	**4**	**CO5**
	SECTION B **(4Qx10M= 40 Marks)**		
Q 6	Differentiate between a prime implicants and no-prime implicants. Also, minimize the following multiple output functions using K-map: $f_1(A,B,C,D) = \sum m(1,2,3,5,7,8,9) + d(12,14)$ $f_2(A,B,C,D) = \sum m(0,1,3,4,6,8,9) + d(10,11)$ $f_3(A,B,C,D) = \sum m(1,3,5,7,8,9,12,13) + d(14,15)$	**2+8**	**CO1**
Q7	Obtain the minimal expression for $f = \sum m(1,2,3,5,6,7,8,9,1213,15)$ using the Tabular (Quine- Mc-Cluskey) method.	**8+2**	**CO2**
Q8	Design and analyze the operation of 8-4-2-1 binary coded decimal (BCD) to 7-segment decoder.	**10**	**CO3**

Q9	The 2125A is a static RAM IC that has a circuitry of 1Kx1, one active-LOW chip select, and separate data input and output. Show how to combine several 2125A ICs to form a 1Kx8 module.	**10**	**CO5**
SECTION-C (2Qx20M=40 Marks)			
Q 10	Design and analyze the 3-bit Gray code counter using the T-flip flop. Implement the state diagram and logic diagram (using basic logic gates and flip-flops) to understand the operation. Write the suitable application of it also. **OR** Implement a 3-bit ripple counter using D flip-flops. Also, draw and analyze timing diagram considering the propagation delay (no skipping states)	**20**	**CO4**
Q11	**Attempt all the parts:** **(a)** Elucidate the (i) dynamic and static memory (ii) Magnetic memory **(b)** It is desired to combine several 1K×8 PROMs to produce a total capacity of 4K×8. How many Chips are required? Design and analyze the arrangement.	**6+14**	**CO5**