Name:

Enrolment No:

UPES

End Semester Examination, May 2023

Course: Analog and Digital Electronics **Semester: II**

Program: B.Tech Mechatronics **Time : 03 hrs.**

Course Code: ECEG 2030 **Max. Marks: 100**

Instructions:

SECTION A

(5Qx4M=20Marks)

S. No.		Marks	CO
Q1.	Write about the classification of multistage amplifiers.	**4**	**CO1**
Q2.	Draw the construction of 555 timer and indicate the pins.	**4**	**CO2**
Q3.	Define CMRR. Determine the output voltage for the OP-amp if v_{in1}=5V and V_{in2} =7V and Gain A= 200000.	**4**	**CO3**
Q4.	Obtain the dual and complement of the following Boolean expression. F=A'B+A'BC'+A'BCD+A'BC'D'E Write about the self-complementing codes and its significance.	**4**	**CO4**
Q5.	Write the difference between latch and flip-flop. Draw the diagram of RS-Latch using NOR-NOR gates.	**4**	**CO5**

SECTION B

(4Qx10M= 40 Marks)

Q6.	Discuss Class A amplifier's design and list out the advantages and disadvantages.	**10**	**CO1**
Q7.	Consider a 555 timer as astable multi-vibrator. For R_A = 6.8 kΩ, R_B = 3.3 kΩ and C = 0.1 µF, calculate (a) t_{high}, (b) t_{low} (c) free running frequency and (d) duty cycle [where t_{high}, & t_{low} are the time duration of Logic High and Logic Low]	**10**	**CO2**
Q8.	(a)Simplify the logic function f(w, x, y, z)= $\sum$ (0,1,2,5,8,9,10,15) using K-Map and realize with NAND GATES . (b)Construct a hamming code for data string 1101, using even parity.	**5+5**	**CO3**

	Locate the error if during receiving the message there was error at 5th position.		
Q9.	Define data selector. Design a 16x1 multiplexer using 4x1 multiplexers only.	**10**	**CO4**
SECTION-C **(2Qx20M=40 Marks)**			
Q10	a)Design a combinational circuit which implements the function $F_1(A,B,C,D,E)=\Sigma m(0, 2, 5, 7, 9, 11,12,13, 17,19, 22,28, 29,)$ using multiplexer b) Implement logic functions $F_1(A,B,C,D)=\Sigma m(0, 2, 7, 9, 11,13)$; $F_2(A,B,C,D)=\Sigma m(0, 2, 7, 9, 11,13)$ using decoder	**10+10**	**CO4**
Q11	(a)Write about the types of triggering in the sequential circuits. (b)Design a mod-10 synchronous counter using T Flip Flop OR (a)Elucidate the following Shift Registers, (i) Parallel In Serial Out (ii) Serial In Serial (b)Design a Ripple counter using T Flip Flop with clock time period as 15 sec and with edge triggering.	**6+14**	**CO5**