


Name:	 UPES UNIVERSITY WITH A PURPOSE
Enrolment No:	

UNIVERSITY OF PETROLEUM AND ENERGY STUDIES
End Semester Examination, December 2020

Course: Digital System Design

Semester: III

Program: B. Tech ECE

Time 03 hrs.

Course Code: ECEG 2028

Max. Marks: 100

Instructions: Answer all the questions.
Diagrams must be neat and clean.

SECTION A

Each Question will carry 5 Marks

Instruction: Complete the statement / Select the correct answer(s)/write a few words

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Q 1	Convert the following octal numbers to binary equivalent i) 762.231 ii) 723.301	CO1
Q 2	Represent the following decimal numbers in 2's complement representation using 8 bits i) -44 ii) 64	CO1
Q 3	What are the problems in asynchronous circuits?	CO2
Q 4	Find the Gray codes for the following binary numbers: a) 11001100 b) 0101110	CO1
Q5	Define the following terms : i) Fan in ii) Fan out iii) Noise immunity	CO5
Q6	Define the following terms : i) Unipolar Logic Families ii) Bipolar Logic Families	CO5

SECTION B

Each question will carry 10 marks

Instruction: Write short / brief notes

Q 1	Explain CMOS inverter gate and totempole output configuration for a TTL gate.	CO5
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Q 2	Minimize the following logic function using K-Map : i) $Y(A,B,C,D) = \sum m(0,1,2,3,5,7,8,9,11,14)$ ii) $Y(A,B,C,D) = \prod M(0,2,8,9,12,13,15)$	CO2
Q 3	Design a mod 9 ripple counter using T-Flipflop and draw the output waveforms	CO4
Q 4	Implement the following output functions using a suitable PLA $F1(A,B,C,D) = \sum m(3,7,8,9,11,15)$ $F2(A,B,C,D) = \sum m(3,4,5,7,10,14,15)$ $F3(A,B,C,D) = \sum m(1,5,7,11,15)$	CO3
Q 5	Design a sequence generator using J-K flipflop to generate the sequence 0-2-4-5-1-7-6	CO4

SECTION-C

Each Question carries 20 Marks.

Instruction: Write long answer.

Q 1	<p>Design a clocked sequential circuit using J-K flipflop for the state diagram shown in the figure below:</p> <pre> graph LR a((a)) -- "0/0" --> b((b)) b -- "1/0" --> c((c)) c -- "0/0" --> d((d)) d -- "1/1" --> a a -- "1/0" --> a b -- "0/0" --> b c -- "1/0" --> b d -- "0/0" --> c </pre>	CO4
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