Roll No: ----------

UPES

UNIVERSITY OF PETROLEUM AND ENERGY STUDIES

End Semester Examination, December 2017

Program: B. TECH ETIPR	**Semester – III**
Subject (Course) BASIC ELECTRONICS	**Max. Marks : 100**
Course Code : GNEG 282	**Duration : 3 Hrs.**
No. of page/s:3	

SECTION A

Attempt all the questions **4X5 = 20MM**

Q1. Classify the effect of temperature on minority charge carrier concentration and define the mass action law?

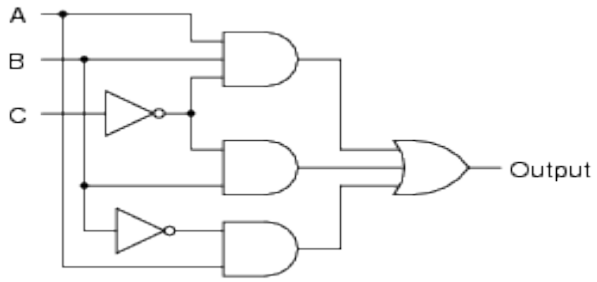
Q2. Consider the given Number system and convert one into another number system?

(a). (A356.B21) = (Base 8)

(b). (1010101011.10011) = (base 16)

Q3. Draw the Reverse and forward characteristics of PN diode and differentiate it with Zener diode?

Q4. Write logical expression for the output and mention the truth table for the given logic diagram below?



Q5. Mention all the bias regions and its applications for common emitter NPN BJT configuration in the output characteristics?

SECTION B

Attempt all the questions **10X4 = 40MM**

Q6. (a) Consider the following Boolean Function *Y*=*A*+(*B*+*C*).(*B*' + A). Reduce the given logical expression and realize the function using NOR gates with truth table?

(b) Determine the current I in the fig 1. Assume Si diodes and forward resistance of diodes to be zero?

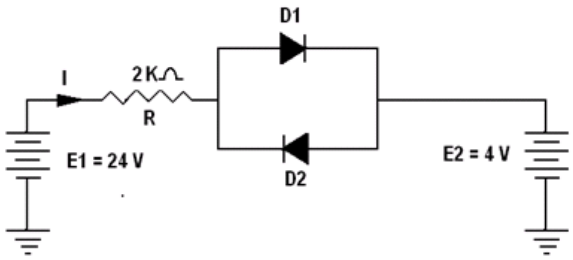


Fig 1

Q7. For the circuit shown below Fig 2 , determine the values of V_L, I_L, I_Z with R_L = 500Ω and R_L = 40Ω. Comment on the operation of the circuit. V_{in} = 25 V, R_S = 250Ω, V_Z = 10 V, P_{Zmax} = 600 mW .

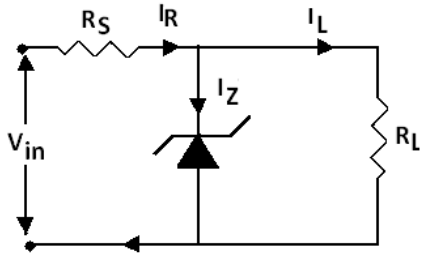


Fig 2

Q8. Consider the half wave Rectifier and compute the derivations for the followings:

(a). True Power dissipated at the load.

(b). The ripple factor and efficiency of the rectifier

(c). Draw input and output waveform

Q9 For the circuit shown below Fig 3 calculate the followings and Draw the Dc load line?

Given: Vcc = 20 V , Rc = 10 k , Rb = 200 ohm , Re = 4 k

(a). Operating point and Region of operation

(b). Output power dissipation

(c). Input characteristics plot

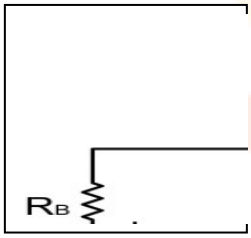


Fig 3

Section C

Attempt all questions **10x2 =40MM**

Q10.Design the Full adder using Half adder by using only NAND gates and mention the logical expression for the outputs with the truth table? Design the logic circuit using Full adder using half adder for addition of two 8 bit numbers?

Q 11. Design a voltage divider bias circuit for an amplifier such that $R1 = 20R2$, and $RE = 2\ K\Omega$. If $VCC = 15\ V$. Consider the Collector current flowing in the circuit = 10mA and current gain =100
(R2 is connected at base to ground).

(a) For VCE = 0.3 V
(b) For VCE = 0.5V

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SECTION A:

Attempt all the questions 4X5 = 20MM

Q1. Consider the given Number system and convert one into another number system?

a. (AA353.BF2) = (Base 8)

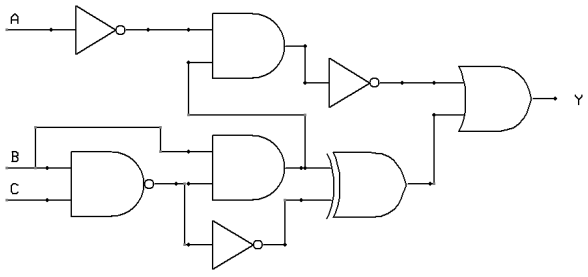
b. (1010101011.10011) = (base 8)

Q2. Analyze the working principle of half wave rectifier and clearly mention input and output `waveform with its working parameters?

Q3. Classify the effect of Doping on minority charge carrier concentration and define the mass action law?

Q4. Write logical expression for the output and mention the truth table for the given logic diagram below?

A	B	C	Y
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	



Q5. Mention all the bias regions and its applications for common base NPN BJT configuration in the output characteristics?

SECTION B

Attempt all the questions **10X4 = 40MM**

Q6. A common emitter fixed bias circuit is subjected to a temperature change from 25 *C* to 50 *C*. The current gain β=100 at 25*C* and 50 at 75*C*. Determine the percentage change in operating values (*VCE* and *IC*) over this temperature change. Neglect any change in *VBE* and the effects on any leakage current. consider *VCC*=20 *V*, *RB*=100 *k*Ω, *RC*=560 Ω.

Q7. Consider the Half wave Rectifier discussed in the class and compute the followings:

(a) True Power dissipated at the load.

(b) The ripple factor and efficiency of the rectifier

(c) Draw input and output waveform

Q8 For the circuit shown below Fig 2 calculate the followings and Draw the Dc load line?

Given : Vcc = 15 V , Rc = 20 k , Rb = 100 ohm , Re = 10 k

(a) Operating point and Region of operation

(b) Output power dissipation

(c) Input and output characteristics plot

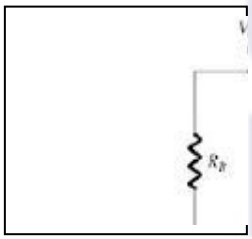


Fig 2

Q9. (a) Consider the following Boolean Function *Y*=*A*+(*B*+*C*).(B' + A.B). Reduce the given logical expression and realize the function using NAND gates with truth table?

(b) Determine the currents I_1, I_2, I_3. Use simplified model. In fig 3

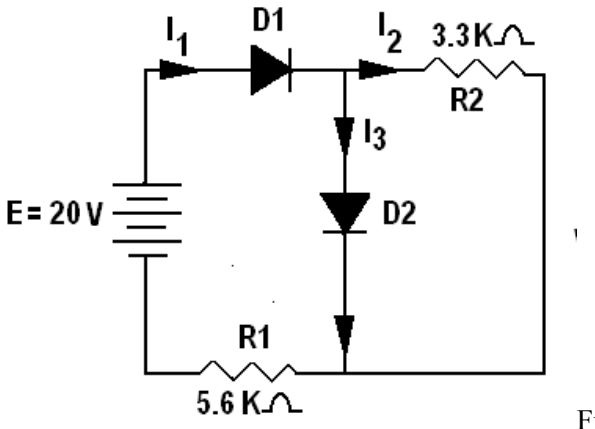


Fig 3

Section C

Attempt all questions **10x2 =40MM**

Q10.Design the Full adder using Half adder by using only NOR gates and mention the logical expression for the outputs with the truth table? Design the logic circuit using Full adder for addition of two 10 bit numbers?

Q 11. Design a voltage divider bias circuit for an amplifier such that *R*1= 10R2, and *RE*=1 *K*Ω. If *VCC*=20 *V*. Consider the Collector current flowing in the circuit = 10mA and current gain =50
(R2 is connected at base to ground).

(c) For VCE = 0.2 V
(d) For VCE = 0.6V