Set-I

Roll No: ----------

UNIVERSITY OF PETROLEUM AND ENERGY STUDIES

End Semester Examination, December 2017

Program: B.Tech-CS+ All IBM branches + Cyber Law **Semester – III**
Subject (Course): Computer System Architecture **Max. Marks : 100**
Course Code : INFO 119 **Duration : 3 Hrs**
No. of page/s: 3

Section -A

Answer the all following questions **4 * 5 = 20M**

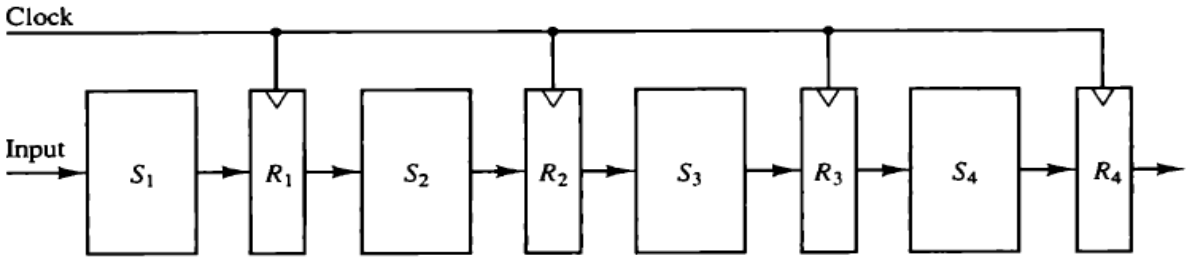
1. Explain about interrupt nesting and software poll with suitable diagram. 5M
2. State how read and write operations executes through hazards, explain with assembly operations. 5M
3. Explain how memory mapped IO and isolated IO executes with status operations. 5M
4. Explain about BRP, BRN, BRO, BRZ, SBR, ISR 5M

Section -B

Answer the all following questions **4 * 10 = 40M**

5. A. Explain about data transfer techniques with the help of a suitable diagram. 5M
   B. Explain the major functions of an IO module. 3M
   C. Construct NAND based SR-latch 2M
6. A. Consider the arithmetic statement X = (A + B) * (C + D). Write down the Three-Address, Two-Address, One-Address and Zero-Address Instruction for this statement. 5M
   B. Explain operations in IO commands 3M
   C. Why Combinational Circuits 2M
7. A non-pipeline system takes 100ns to process a task. The same task is fed for processing to a 4-stage pipeline with clock cycle time of 25 ns. The propagation time of registers

R1, R2, R3 and R4 is zero.



a. Determine the number of clock cycles that it takes to process 200 tasks in this 4-stage pipeline.
b. Determine the speedup ratio of the pipeline for 200 tasks.
c. What is the theoretical maximum speedup that could achieved with this pipeline system over a non-pipelined system?
d. If the propagation delay time of registers R1,R2,R3,R4 is 10ns,30ns,40ns,20ns respectively ,then find the speedup ratio of the 4 stage pipeline for 200 tasks. (2+3+2+3)M

8. A two-word instruction is stored at location 300. The address field has the value 400. A processor register R1 contains the value 200. Evaluate the effective address if the addressing mode of the instruction is (2+2+2+2 +2)M
    a. Direct
    b. Immediate
    c. Relative
    d. Register Indirect
    e. Index with R1 as index register

Section -C

Answer the all following questions **2 * 20 = 40M**

9. A. Define Associative Memory. Establish the match logic for one complete word of Associative Memory with logic diagram. State the advantage of Associative Memory. 7M

B. A computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers and an address part:

I. How many bits are there in the operation code, the register code part and the address part?

II. Draw the instruction word format and indicate the number of bits in each part

III. How many bits are there in data and address inputs of the memory. (3+ 3+ 2)M

C. Explain the conflicts/hazards in Instruction pipeline. 5M

10. A. What are the different types of fields that are part of an instruction? Explain. 2.5M

B. Point out the characteristics of the RISC & CISC architecture with neat diagrams. 5M

C. Illustrate this expression ((15 ÷ (7 − (1 + 1))) × 3) − (2 + (1 + 1)) with Stack memory (explain with RPN notation, procedure flow for PUSH & POP operations and corresponding assembly code). 10M

D. What is a common Bus? How this common bus implemented in IO operations 2.5M

Set-II

Roll No: ----------

UNIVERSITY OF PETROLEUM AND ENERGY STUDIES

End Semester Examination, December 2017

Program: B.Tech-CS+ All IBM branches + Cyber Law — **Semester – III**
Subject (Course): Computer System Architecture — **Max. Marks : 100**
Course Code : INFO 119 — **Duration : 3 Hrs**
No. of page/s: 3

Section A (Attempt All)

4 * 5 = 20M

Question 1: The following memory units specified by the number of words times the number of bits per word. How many address lines and input-output data lines needed in each case? (a) 4K x 16, (b) 2G x 8, (c) 16M x 32, (d) 256 K x 64. Also, give the number of bytes stored in the memories listed. 5M

Question 2: Construct SR-FF to JK-FF with NAND gates 5M

Question 3: Differentiate combinational Circuits and sequential Circuits 5M

Question 4: Solve the following 5M

$(F9DA.78C)_{16}$ - $()_{10,}$ $(01010101.910178)_{10} - ()_2$

Section B (Attempt All)

4 * 10 = 40M

Question 5: Explain the complete procedure of address Sequencing (address calculation) of microinstructions present in control memory in a microprogrammed control unit with the help of suitable diagram 10M

Question 6: 24-bits specify an address space and the corresponding memory space specify an address space by 16 bits.

a. How many words are there in the address space?

b. How many words are there in the memory space?

c. If a page consists of 2K words, how many pages and blocks are there in the system?

d. Write down short-note on replacement algorithm of cache memory. (2+2+2+4)M

Question 7: Explain the following

A. Super scalar Processing 2M

B. Asynchronous & Synchronous pipeline 4M

C. Hardwired & Microprogrammed control units 4M

Question 8: A. Describe the importance of Nano control memory 2M

B. what is the difference between Nano instruction and Microinstruction 3M

C. Describe Nano instruction format of Qm-1? 3M

D. Explain how Nano programming reduces the total size of required control memory. 2M

Section C (Attempt Any Two)

2 * 20 = 40M

Question 9: A. Explain the differences between hardwired control and microprogrammed control units with their process execution architectures 10M

B. A system uses a control memory of 1024 words of 32 bits each. The microinstruction has three fields as select field, address field and micro operation field. The micro operation field has 16 bits.

I. How many bits are there in the branch address field and the select field?

II. If there are 16 status bits in the system, how many bits of the branch logic used to select a status bit?

III. How many bits left to select an input for the multiplexers?

(3+3+4)M

Question 10: A. Determine the number of clock cycles that it takes to process 200 tasks in a six-segment pipeline. A non-pipeline system takes 50 ns to process a task. The same task can processed in a six-segment pipeline with a clock cycle of 10 ns. Determine the speedup ratio of the pipeline for 100 tasks. What is the maximum speedup achieved?

10M

B. Answer the following

I. How many 128 × 8 RAM chips are required to provide a memory capacity of 2048 bytes?

II. How many lines of the address bus must use to access 2048 bytes of memory?

III. How many of these lines will be used to address each chip and how many lines will be used to select the chips?

IV. What is Flash Memory? Differentiate between EEPROM and EPROM.

(2+2+2+4)M

Question 11: A. Explain 5-stage pipelined processor has Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Perform Operation (PO) and Write Operand (WO) stages. 10M

B. the IF, ID, OF and WO stages take one clock cycle each for any instruction. The PO stage takes one clock cycle for ADD and SUB instructions, three clock cycles for MUL instruction, and 6 clock cycles for DIV instruction respectively. Operand forwarding used in the pipeline. What is the number of clock cycles

needed to execute the following sequence of instructions?

10M

Instruction	Meaning of instruction
MUL R2 ,R0 ,R1	R2 ← R0 *R1
DIV R5 ,R3 ,R4	R5 ← R3/R4
ADD R2 ,R5 ,R2	R2 ←R5+R2
SUB R5 ,R2 ,R6	R5 ← R2-R6