UNIVERSITY OF PETROLEUM AND ENERGY STUDIES

UPES

End Semester Examination, December 2017

Program: B Tech.(Mechatronics Engineering) **Semester –III**
Subject (Course): Analog and Digital Electronics **Max. Marks : 100**
Course Code :GNEG291 **Duration: 3 Hrs**
No. of page/s:

NOTE: Attempt all questions

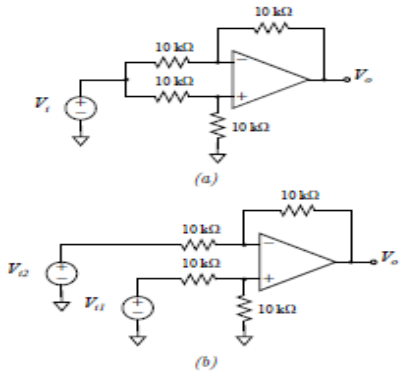
Part A **[5×4 = 20]**

1. Simplify the Boolean Expression F(W,X,Y,Z) = ∑(1,3,7,11,15) + ∑d(0,2,5) with the help of K-Map.
2. Realize EX-NOR gate from NAND Gate and draw its truth table by verifying the Boolean expression.
3. Convert from one number system to another.
   a. $(37.4)_{16}$ = (?)$_{10}$
   b. $(ECE)_{16}$ = (?)$_{10}$
   c. $(754.23)_{8}$ = (?)$_{2}$
   d. $(FACE)_{16}$ = (?)$_{8}$
4. In a 4-bit ripple counter propagation delay of ripple counter is 25 ns then maximum clock frequency that can be applied to the counter is…….?

Part B **[10×4 = 40]**

5. Implement 4-bit Look Ahead Carry Adder with the help of AND-OR-EXOR gates and if all logic gates have propagation delay, then calculate the delay at Carry and Sum.
6. Implement f(A,B,C)= ∑m(0,1,5,6,7) using 4x1 MULTIPLEXER with A and C as control variable.
7. Develop Full Adder using 3x8 Decoder and draw its logic diagram.

8. Determine V_{out} for the two connections shown in below Figure. Assume V_1 = 3V, V_a =2V and V_b = 3V.



Part C **[2×20 = 40]**

9. A clocked X-Y flip flop is defined with two inputs, X and Y is in addition to the clock input. The flip flop functions as follows:

If XY=00, the flip flop changes state with each clock pulse.

If XY=01, the flip flop state Q becomes '1' with the next clock pulse.

If XY=10, the flip flop state Q becomes '0' with the next clock pulse.

If XY=11, the change of state occurs with the clock pulse.

a. Write a truth table for the XY flip flop.
b. Write the Excitation tables for the XY flip flop.
c. It is desirable to convert a J-K flip flop into X-Y flip flop by adding some external gates, if necessary. Design a circuit to show how you will implement X-Y flip flop using J-K flip flop.

10. Design a circuit using op-amp to produce a square wave output whose output does not have any stable state and the Output has two Quasi-Stable states where output keeps on changing its own from 1state to another state and Vice Versa.

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Roll No: ----------

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   b. $(FACE)_{16} = (\ ?\ )_{10}$
   c. $(754.23)_{8} = (\ ?\ )_{2}$
   d. $(CAD)_{16} = (\ ?\ )_{8}$
2. Simplify the Boolean Expression $F(W,X,Y,Z) = \sum(1,3,7,11,15) + \sum d(0,2,5)$ using K-Map.
3. Realize EX-NOR gate from NAND Gate and draw its truth table by verifying the Boolean expression.
4. In a 4-bit ripple counter propagation delay of ripple counter is 25 ns then maximum clock frequency that can be applied to the counter is…….?

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5. Implement 4-bit Look Ahead Carry Adder with the help of AND-OR-EXOR gates and if all logic gates have propagation delay, then calculate the delay at Carry and Sum.

6. Implement $f(A,B,C)= \sum m(0,1,5,6,7)$ using 4x1 MULTIPLEXER with A and C as control variable.

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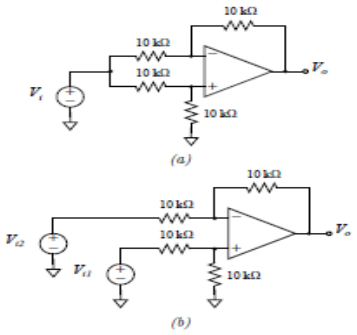

8. Develop Full Adder using 3x8 Decoder and draw its logic diagram.

Part C **[2×20 = 40]**

9. Design a circuit using op-amp to produce a square wave output whose output does not have any stable state and the Output has two Quasi-Stable states where output keeps on changing its own from 1state to another state and Vice Versa.
10. A new clocked X-Y flip flop is defined with two inputs, X and Y is in addition to the clock input. The flip flop functions as follows:
    If XY=00, the flip flop changes state with each clock pulse.
    If XY=01, the flip flop state Q becomes '1' with the next clock pulse.
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