UPES

UNIVERSITY OF PETROLEUM AND ENERGY STUDIES

End Semester Examination, December 2017

Program: B.Tech/PSE   Semester –III
Subject (Course): Analog & Digital Electronics   Max. Marks   : 100
Course Code   : ELEG226   Duration   : 3 Hrs
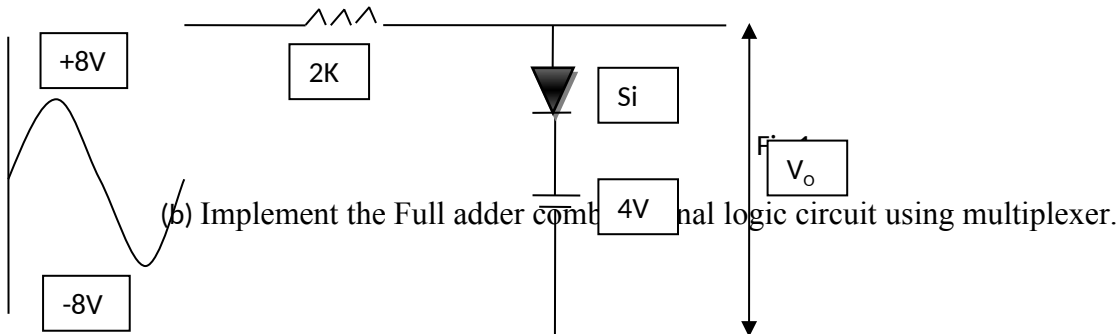**No. of page/s:02**

Section (A)   20 Marks

All questions are compulsory and carry equal marks.

1) In a transistor,β=45 the voltage across 5kΩ resistance which is connected in the collector circuit is 5Volts.Find the base current

2) Draw and explain the block diagram of an N-bit parallel adder/substractor   and explain its limitations.

3) Draw the logic diagram of a SR latch using NOR gates. Explain its Operation using Excitation table.

4) (a) Perform the following operations by using 2's complement method   [2+2+1]
         i) 46-23 ii) 21-42
     (b) Perform the following operations by using 1's complement method
         i) 42-22 ii) 20-42
      (c) Convert   the gray code 1011001100 into its binary

Section (B)   40 Marks

All questions are compulsory and carry equal marks.

1) (a) Sketch the output waveform for the following network fig 1 and write down the applications of clipper circuit.

+8V

-8V

2K

Si

4V

V$_o$

(b) Implement the Full adder combinational logic circuit using multiplexer.

2) Draw and explain typical output characteristics of NPN transistor in CE configuration. Label all variables and indicate active, cutoff and saturation regions.

3) Describe the voltage divider biasing circuit in detail. How stabilization of operating point is achieved by the biasing method? Why it is so popular.

4) Design a 4-bit universal shift register and draw the circuit with the given mode of operation table 1

S1	S0	Operation
0	0	Parallel
0	1	Shift right
1	0	Shift left
1	1	Inhibit clock

Table 1

(or)

5) Design a 4-bit Asynchronous up/down counter

Section(C) 40 Marks

Attempt any two questions and each carry equal marks.

10) (a) Convert a D flip flop into SR flip flop and JK flip flop?   [13+7]

(b) Design a 2-bit magnitude comparator along with the circuit diagram.

11) (a) Obtain the minimal expression for $F==\sum m(1,2,3,5,6,7,8,9,12,13,15)$ using the using Quine- Mc-Cluskey method   [13+7]

(b) In a Silicon transistor circuit with a fixed bias, VCC=9V, RC=3KΩ, RB=8KΩ, β=50, VBE=0.7V. Find the operating point and Stability factor.

12) (a) For the circuit shown below Fig 2 determine the values of V_L, I_L, I_Z with $R_L = 200\Omega$ and $R_L = 50\Omega$. Comment on the operation of the circuit. Vin = 20 V, $R_S = 220\Omega$, $V_Z = 10$ V, PZmax = 400 mW .   [10+10]
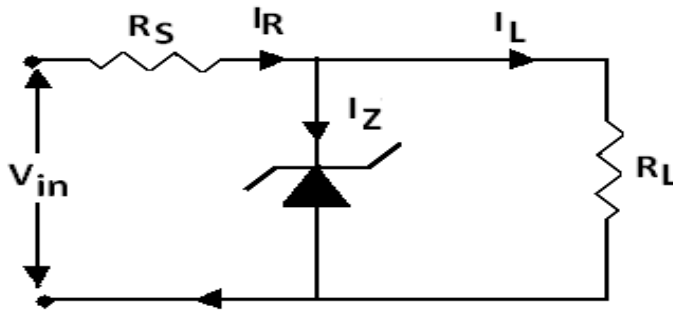

Fig 2

(b) Design a neat circuit diagram of a 4-bit bidirectional shift register using D- flip flop having right and left data inputs and mode control M such that M=0 left shift, M=1 right shift

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Section (A)   20 Marks

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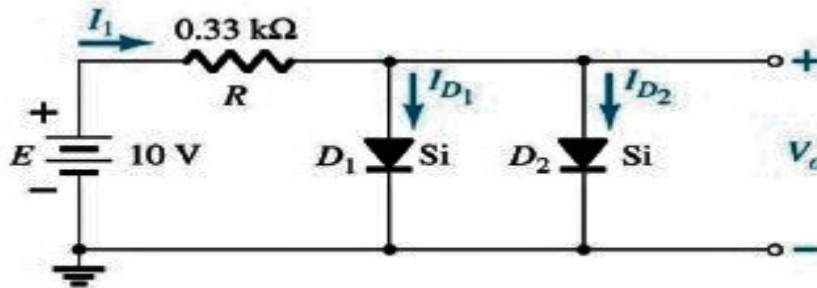1) Determine V_o, I_1, I_{D1} and I_{D2} for the parallel diode Shown below Fig 1

Fig 1

2) Implement a half subs tractor using 4*1 Multiplexer.
3) In what way the temperature variation affects the operating point of a transistor.
4) Perform the subtraction using 1's complement and 2's complement methods.
   (i)11010 – 10000 (ii)11010 – 1101 (iii)100 - 110000

Section (B)   40 Marks

All questions are compulsory and carry equal marks.

5) Describe the various methods used for transistor biasing. State their advantages and disadvantages.

6) Draw the JK master- slave flip- flop and explain how to eliminate the race around condition.

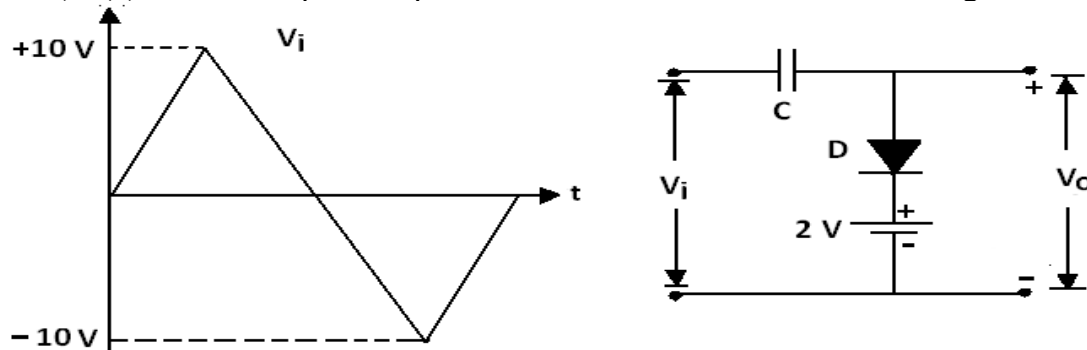7) (a) Draw and explain output waveforms of the circuit as shown in fig-2   [6+4]

Fig-2

(b) Draw and explain the crystal diode equivalent circuits and models.
   (i) Approximate Model (ii) Simplified model (iii) ideal diode.

8) Design a Mod 12 counter using D- flip- flop
       (or)

9) Draw the explain typical output characteristics of NPN transistor in CB configuration. Label all variables and indicate active, cutoff and saturation regions.

Section(C) 40 Marks

Attempt any two questions and each carry equal marks.

10) (a) A silicon transistor of NPN type is used in voltage divider bias with $\beta = 100$, RC = 10KΩ, RE = 1.5KΩ, R1 = 39KΩ, R2 = 3.9KΩ and VCC = 22V. Find the Thevinin voltage, Thevinin resistance, Base current, Collector current, Q-point and stability factor.
    (b) Design a 4 bit gray to binary converter using truth table-maps, and logic circuits.

[13+7Marks]

11) (a) Convert the following i) JK flip-flop to T flip-flop ii) RS flip-flop to D flip-flop.
     (b) Design a 4-bit down/up ripple Asynchronous counter.

12) Solve the following using Quine Mc- Clusky method
     $F(x1, x2, x3, x4, x5) = \sum(0,1,4,5,6,7,8,10,14,17,18,21,29,31)$.