Roll No: --------------------------

UNIVERSITY OF PETROLEUM AND ENERGY STUDIES

End Semester Examination, December 2017

Program: B Tech ICE | **Semester – V**
Subject (Course): Operational Amplifiers and Applications | **Max. Marks : 100**
Course Code : ICEG311 | **Duration : 3 Hrs**
No. of page/s: 3

Instructions:

- Attempt all questions
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- Strike off all unused blank pages

Section – A (5x4 = 20 Marks)

1. Write short notes on virtual ground concept.
2. A particular inverting amplifier with nominal gain of -100 uses a non-ideal op-amp with RF = 100 kΩ and R1 = 10 kΩ resistors. The output is found to be +9.09 V with the input grounded. Estimate the value of the input offset voltage.
3. What is the function of op-amp comparator circuit? List out at least four applications.
4. Define three states in Phased Locked Loop (PLL): free running; capture; phase lock
5. A six-bit A/D converter has a maximum precision supply voltage of 20 V. What voltage change does each LSB represent? What voltage does 100110 represent?

Section – B (5x8 = 40 Marks)

6. Draw the circuits for precision half-wave and full-wave rectifiers, using Op-Amps. Explain their working with the help of waveforms and equations.
7. Draw the block diagrams of the 555 timer Show how 555 can be used as an mono-stable multi-vibrator. Describe the circuit operation with the help of waveforms and derive an expression for the frequency of oscillations

8. Obtain the mathematical expression for the output v_0 in time or frequency domain in circuit shown in **Fig. 1** hence identify the circuit function.

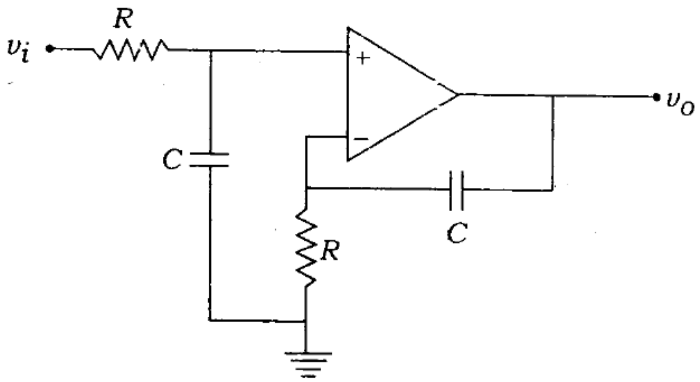

Fig.1

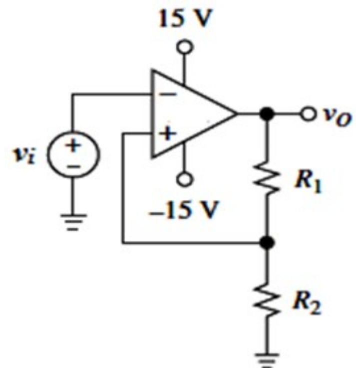

Fig. 2

9. A regenerative comparator (Schmitt Trigger) circuit is shown in **Fig. 2** (i) Derive expressions for upper threshold and lower threshold voltages, V_{UT} and V_{LT} respectively and hence the value of hysteresis voltage V_H. Calculate V_{UT}, V_{LT}, V_H for the given values of R_1 = 27 kΩ and R_2 = 1 kΩ. (ii) A sine wave with 2 V peak-to-peak amplitude and 1 kHz frequency is app lied at the input of the circuit. Plot the input and output waveforms. Vcc = + 15 V

10. What are the advantages of dual-slope A/D converter? Give a schematic diagram of such a converter and explain its operation with the help of timing waveforms.

Section – B (2x20 = 40 Marks)

11. (a) Design a multi-feedback 2^{nd} order low pass filter shown in **Fig. 3** with a cut-off frequency of 1 kHz, a voltage gain of 20 dB and a quality factor (Q) of 5. Given that R_1 = R_2 = 1 kΩ

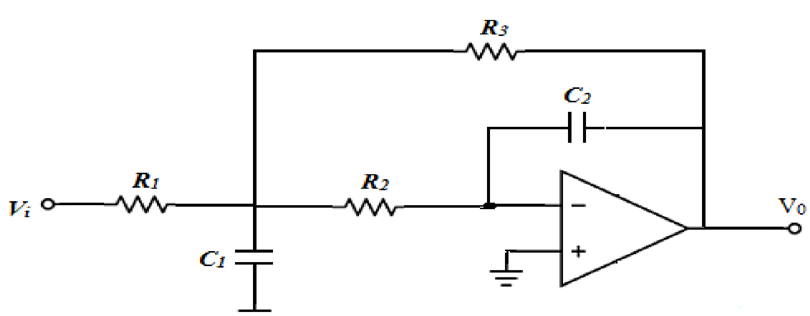

Fig.3

(b) Design a circuit (**Fig. 4**), using one ideal op amp, whose output is $V_O = V_{i1} + 3V_{i2} - 2(V_{i3} + 3V_{i4})$.

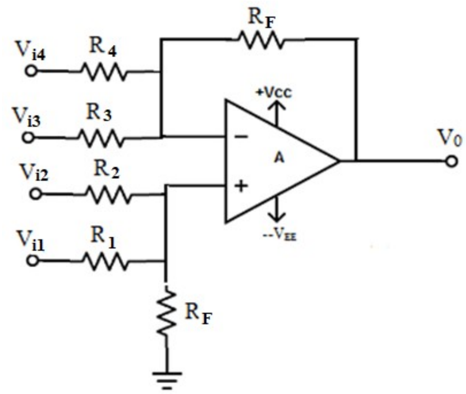

Fig. 4

12. **(a)** Design an astable multi-vibrator using 555 timer for a frequency of 10 kHz and a duty cycle of 60%. Assume C = 0.5 μF

(b) Fig. 5 shows a circuit for a digital-to-analog converter (DAC). The circuit accepts a 4-bit input binary word $a_3a_2a_1a_0$, where a_0, a_1, a_2, and a_3 take the values of 0 or 1, and it provides an analog output voltage V_0 proportional to the value of the digital input. Each of the bits of the input word controls the correspondingly numbered switch. For instance, if a_2 is 0 then switch S_2 connects the 20 kΩ resistor to ground, while if a_2 is 1 then S_2 connects the 20 kΩ resistor to the +5 V power supply. Show that V_0 is given by

$$V_0 = -\frac{R_f}{10}\frac{V_R}{2^n}\left(2^3 a_3 + 2^2 a_2 + 2^1 a_1 + 2^0 a_0\right)$$

Where R_f is in kΩ. Find the value of R_f so that V_0 ranges from 0 to -12 volts.

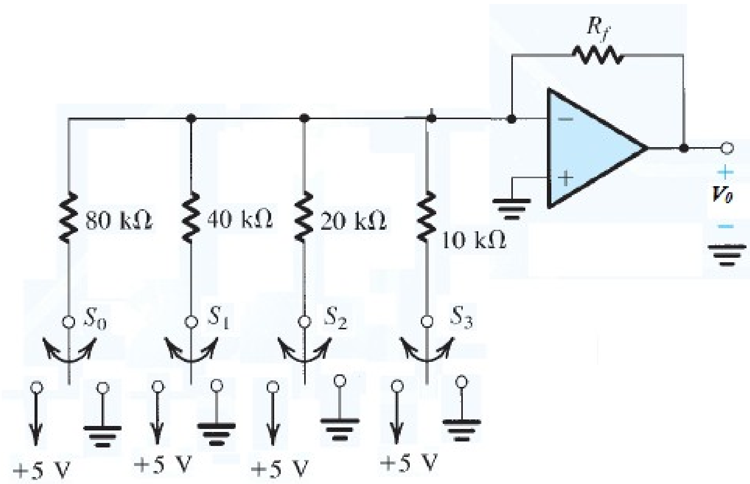

Fig. 5

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Section – A (5x4 = 20 Marks)

1. What are the important features of an instrumentation amplifier?
2. An op amp wired in the inverting configuration shown in **Fig. 1** with the input grounded, having R_2 = 100 kΩ and R_1 = 1 kΩ, has an output dc voltage of –0.4 V. If the input bias current is known to be very small, find the input offset voltage.

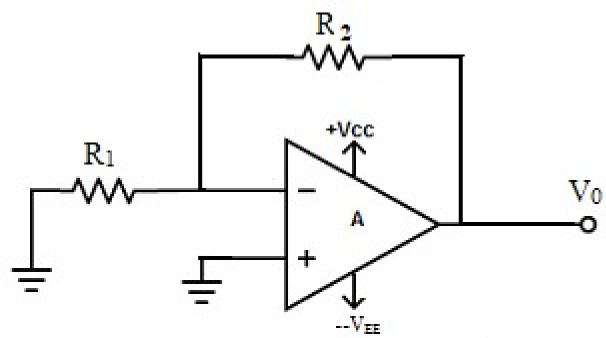

Fig. 1

3. Briefly discuss how the analog multiplier implemented by logarithmic amplifiers.
4. Explain how the triangular waveform can generated from square wave input.
5. Arrange the following A/D converters in order of increasing speed of operation: (i) Successive approximation; (ii) Dual-slope; (iii) Flash; (iv) Single-slope. An 8-bit successive approximation type A/D converter uses a clock frequency of 1 MHz. Calculate the conversion time of the converter.

Section – B (5x8 = 40 Marks)

6. Draw the circuit of an Astable multi-vibrator using OP AMP (s) and explain it working with the help of waveforms. Derive an expression for frequency of oscillations.
7. Draw the 2^{nd} order Sallen key low pass filter circuit diagram. Also, determine the transfer function (V_0/V_i) for this filter.
8. What is the principle of phased locked loop (PLL)? Draw schematic block diagram and explain the same.
9. Draw schematic diagram of an integrated/ dual-slope A/D converter. Explain its working with the help of timing waveforms.
10. Draw and explain the internal schematic circuit diagram of a 555 timer IC.

Section – C (2x20 = 40 Marks)

11. (a) Design the instrumentation-amplifier circuit of **Fig.** to realize a differential gain, variable in the range 1 to 100, utilizing a $2R_1$ = 100 kΩ pot as variable resistor. (Design the second stage for a gain of 0.5).

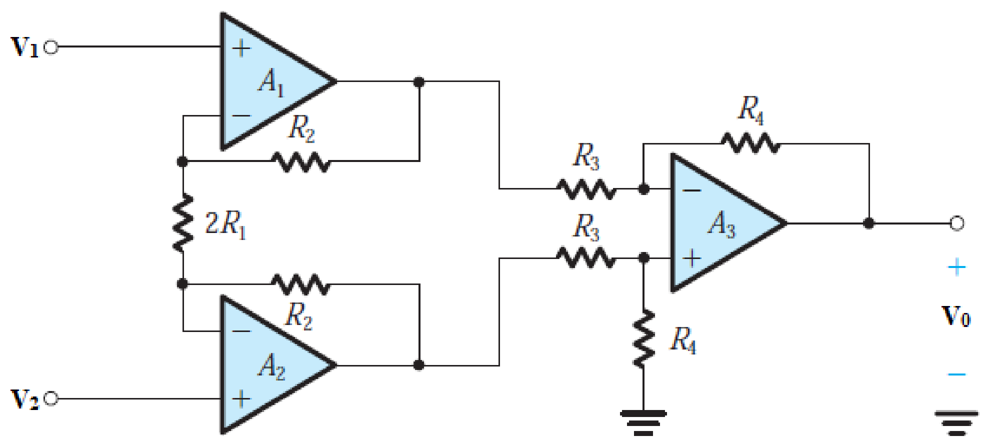

Fig.

(b) To obtain a high-gain, high-input-resistance difference amplifier, the circuit in Fig. employs positive feedback, in addition to the negative feedback provided by the resistor R connected from the output to the negative input of the op amp. Specifically, a voltage divider (R_5, R_6) connected across the output feeds a fraction β of the output, that is, a voltage βV_0, back to the positive-input terminal of the op amp through a resistor R. Assume that R_5 and $R6$ are much smaller than R so that the current through R is much lower than the current in the voltage divider, with results that $\beta \cong \frac{R_6}{R_5+R_6}$.

Show that the differential gain is given by

$$A_d = \frac{V_0}{V_{id}} = \frac{1}{1-\beta}$$

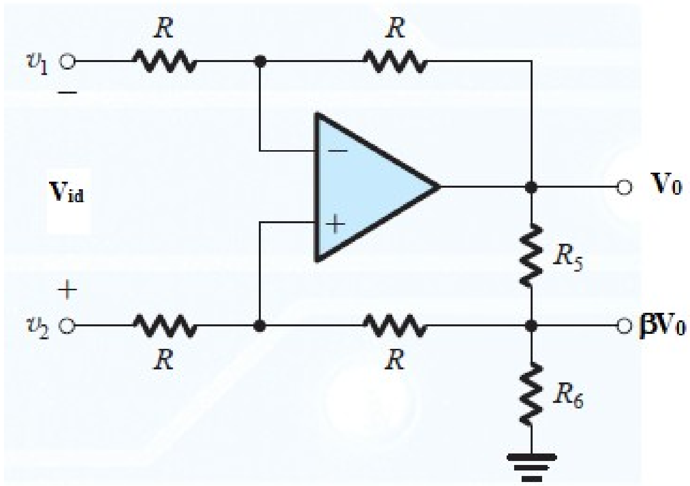

Fig.

Design the circuit to obtain a differential gain of 10. Select values for R, R_5, and R_6, such that $R_5 + R_6 \leq R/100$

12. **(a)** Assume you have a 4-bit Successive Approximation type ADC. For the analog input 0.25V; 1.5 and 1.75 V, show how the SAR would approximate the analog input with relevant diagrams. (Given that the V_{ref} is 4V)

(b) It is required to design a noninverting amplifier with a dc gain of 10. When a step voltage of 100 mV is applied at the input, it is required that the output be within 1% of its final value of 1 V in at most 100 ns. What must the *value of slew rate and frequency* f_t of the op amp be?