Roll No: ----------

UPES

UNIVERSITY OF PETROLEUM AND ENERGY STUDIES

End Semester Examination, December 2017

Program Name: B.Tech (Electronics Engineering) | **Semester – VII**
Course Name : VLSI Design | **Max. Marks : 100**
Course Code : ELEG - 405 | **Duration : 3 Hrs**
No. of page/s: 03

Section-A (4 x 5 = 20 Marks)

Attempt *all* the questions

Q.1 What is ASIC ? List the different abstraction levele of ICs and suggest the suitable examples. [5]

Q.2 Explain the Noise Margin and speed of operation of digital circuits. A logic gate is defined by the following volatge levels

$$V_{OH} = 5\ V$$
$$V_{OL} = 0.2\ V$$
$$V_{IH} = 2.5\ V$$
$$V_{IL} = 0.8\ V$$

Find the noise margin of this gate. [5]

Q.3 Justify the output of the following logic diagram and show the minimum Euler's path. [5]

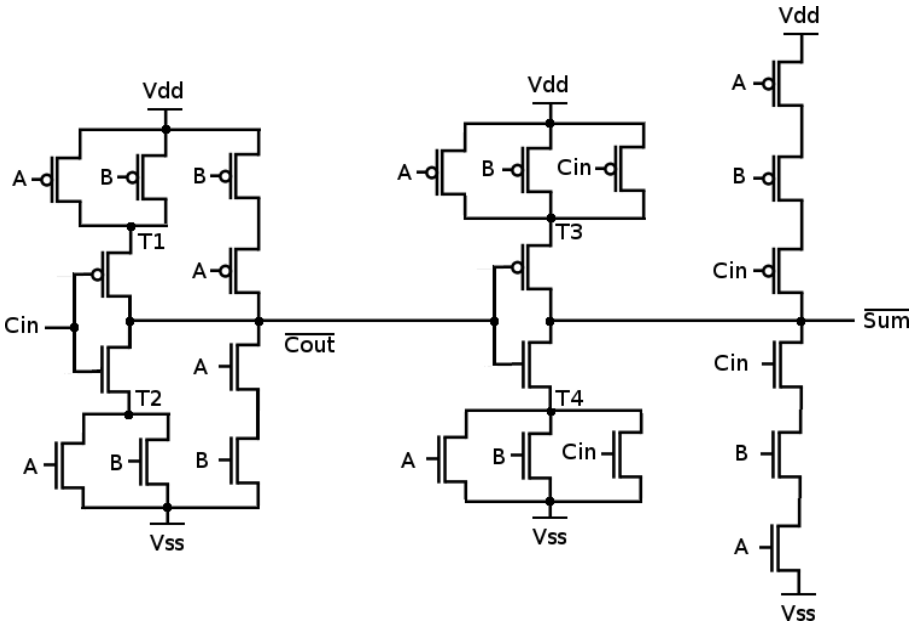

Fig.1 MOS circuit realization

Q.4 Design the falling edge triggered asynchronous 'JK' flip flop using VHDL. [5]

Section-B (4 x 10 = 40 Marks)

Attempt *all* the questions

Q.5 Explain the working of enhancement type NMOS and detail V-I characteristics in all regions. Derive the mathematical expression for the drain current in all the regions. [10]

Q.6 Derive the mathematical expressions to estimate the value of V_{OH}, V_{OL}, V_{IL} and V_{IH} for NMOS inverter circuit and detail the functionality with voltage transfer characteristics with resistive load. [10]

OR

Draw the voltage transfer curve for the CMOS inverter and derive the mathematical expression to estimate the value of V_{OH}, V_{OL}, V_{IL} and V_{IH} for CMOS inverter circuit and detail the functionality.

Q.7 Draw the structure of CPLD (Max Altera 7000) and explain the functionality. Compare the CPLD with FPGA. [10]

Q.8 Draw the FPGA design flow used for synthesis the logic. Draw the architecture of any one of the FPGA and explain the functionality: XC 4000, SPARTAN 3E, Virtex 5. [10]

Section-C (2 x 20 = 40 Marks)

Attempt *any two* the followings

Q. 9 (a) Design the CMOS logic Implementation for the followings

$$Y = \overline{A[B + C(D + E)]}$$

$$Y = \overline{A[BC + DE]}$$

$$Y = \overline{A(B + CD) + E}$$

Calculate the W/L ratio of the transistors involved in the design. [10]

(b) Draw the stick diagram and layout for NMOS inverter, 2 input NAND and 2 input NOR logic, Mark the all layers with exact colour and discuss the functionality to support your answer. [10]

Q.10 (a) Compare the Melay and Moore FSM with examples. [10]

In the project "Traffic Light Control", the fundamental idea is to control the traffic. It can be used to avoid the vehicular collisions and traffic jams. This project is just a one-way traffic controller, although it can be further modified as well. Project will work in a way, it provides the instruction to the driver whether to drive through the intersection or yield at the intersection.

***Control Lights Indication*:** There are three control lights or signals, which will provide the instruction to the driver.

RED Light – instructs the driver to STOP at the intersection.

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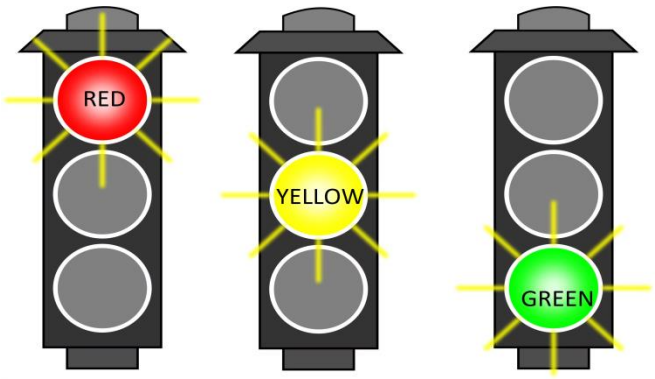

Fig.2 Traffic Light Controller

Fig. 2 presents the conditions of traffic light controller. Develop the HDL code to control the traffic intensity from one side. Also draw the state diagram show the test cases to test the design

(b) Identify the waveform shown in fig. 3 and draw the logic diagram and truth table for the same chip. Develop the VHDL code for the IC using dataflow and behavioral model. [10]

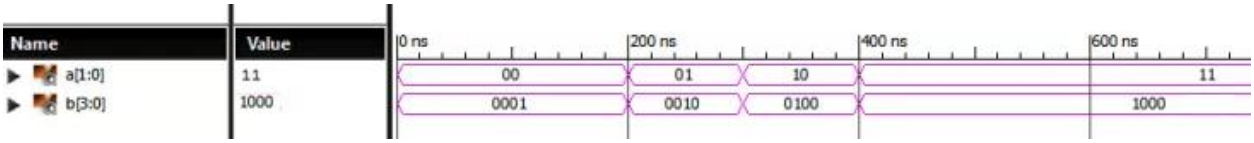

Fig.3 Xilinx ISim Waveform

Q.11 (a) Compare the all PLD technology and realize the following functions using all technology at gate level and N-MOSFT level. [10]

$$F_1 = wxyz + \bar{w}xyz + \bar{w}xyz + wx\bar{y}\bar{z}$$

$$F_2 = wxyz + \bar{w}xyz + w\bar{x}yz + w\bar{x}y\bar{z}$$

$$F_3 = wxyz + +\bar{w}x\bar{y}z$$

$$F_4 = w\bar{x}y\bar{z} + \bar{w}xyz + \bar{w}xy\bar{z} + w\bar{x}yz$$

(b) Draw the cross section view of CMOS under fabrication process. List the all steps required to fabricate the CMOS chip using N-well and P- Well process. Detail the complete operations required to fabricate the same chip. [10]

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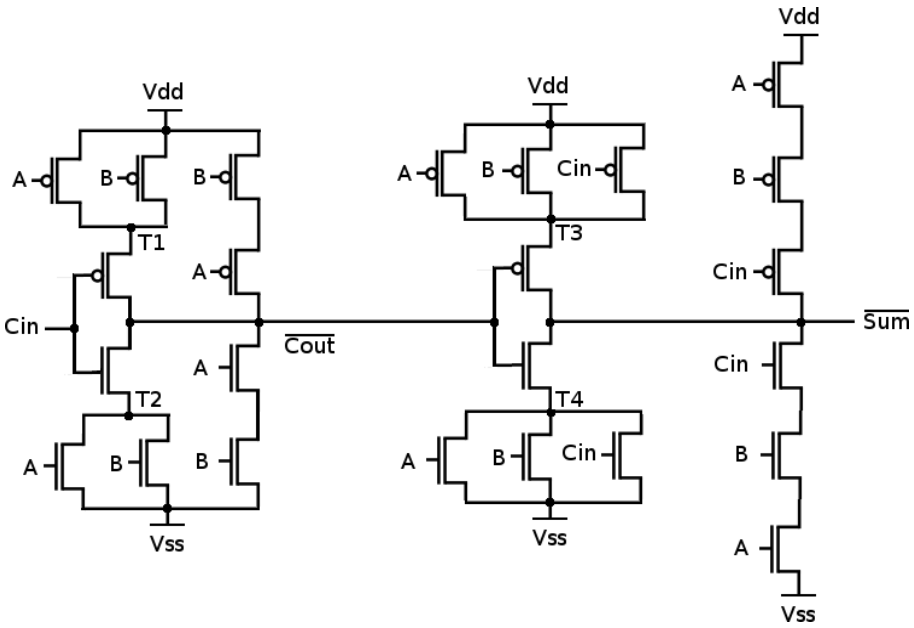

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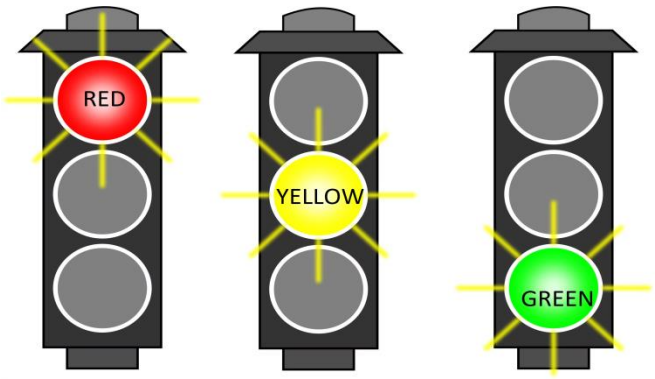

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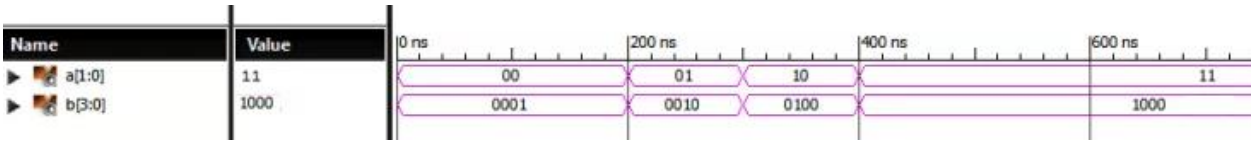

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