Chapter 6

Proposed Tracking Loop Enhancements for Mitigating Signal Interference

6.1 INTRODUCTION

Literatures, mitigation techniques, channel modeling which was studied in the previous chapter were related to the conventional implementation of the OFDMA system without considering FFT window positioning in the presence of Interference. Our approach is also to mitigate the signal interference by using FFT window positioning in the presence of interference. To develop and design the proposed technique for the mitigation of interference we make use of International telecommunication Union (ITU) channel models and observe the power delay profiles at a given instance of time and farrow filters are used to provide the delay and shift the FFT window according to the delay. The performance evaluation is carried out in two cases; where OFDMA is implemented without considering any delays and the other is to make the use of delays provided by the ITU in random cases as provided in appendix A and delay the FFT process until all the symbols have been arrived at the receiver. The reason having two cases is to follow the guidelines provided by [85].

This chapter is organized as follows: section 6.2 gives the overview of the hardware on which the results were carried out i.e. vertex-5 Xilinx FPGA board and its User Constrained File pin detail and section 6.3 gives the overview of experimental setup and the test cases with chipscope followed by the section 6.4 RTL view, section 6.5 simulation results and analysis, section 6.6 synthesis results of proposed technique of OFDMA and section 6.7 gives the hardware implantation of OFDMA. Section 6.8 brings out the consideration and analysis of overall parameters of the system and SNR vs BER results of both conventional OFDMA and FFT window positioned OFDMA and section 6.9 gives the detail report of device utilization and timing synthesis and section 6.10 summarizes the chapter.

6.2 SYNTHESIS TOOL

The synthesis is carried out on the Xilinx Vertex-5 XC5VLX130T FPGA board manufactured by the Digilent Company as shown in the Fig.5.1. The detail descriptions regarding this FPGA like flash memory, Universal Serial Bus (USB), system clock generator etc. can be found in [86], [87] and [88]. It has two XCF32P flash ROMs for sorting large device configurations of 32Mbyte each, 64 bits wide 256 Mbyte DDR2 modules compatible with Embedded Development Kit(EDK) supported IP and drivers.it has 32-bit synchronous zero bus turnaround(ZBT) SRAM and Intel P30 strata flash.

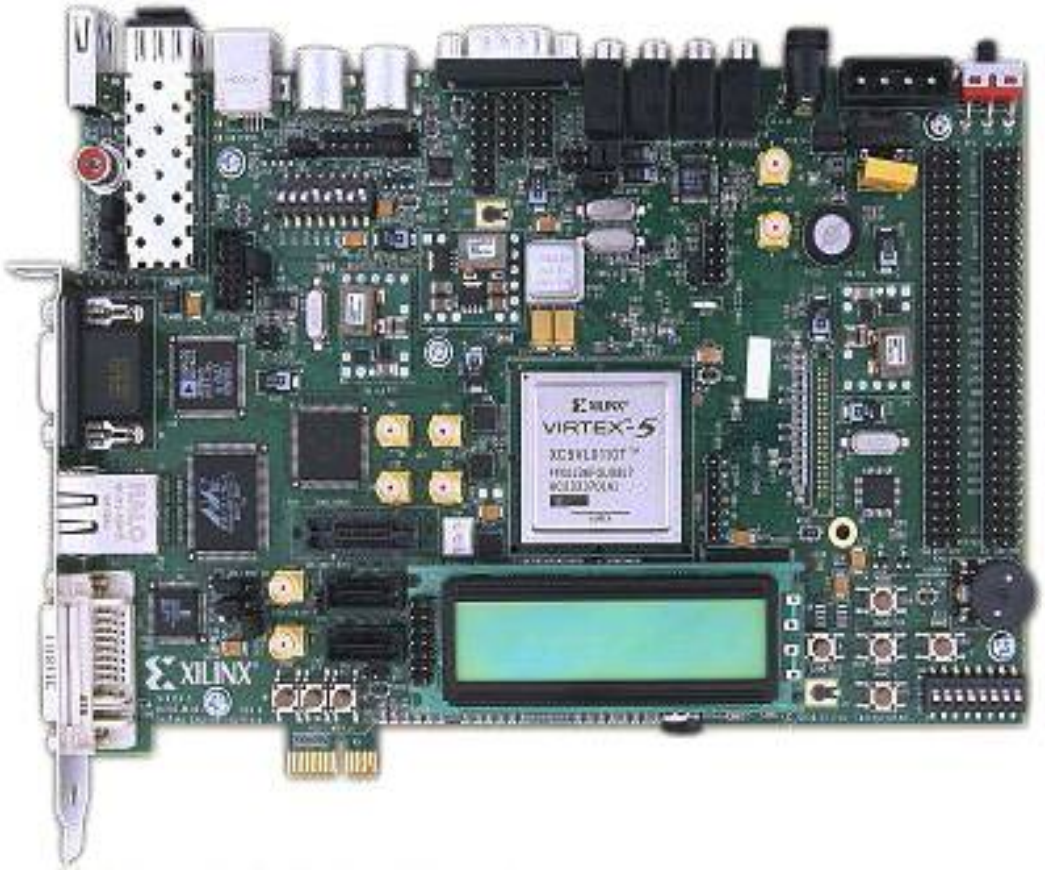

Fig.6.1. Pictorial view of vertex-5 FPGA board

The User Constrained Files (UCF) pins for allocating clock, reset and FFT index details are given in the Table 6.1.

Table 6.1 The User Constrained Files pin details

NET "inputclock" LOC = "C9" | IOSTANDARD = LVCMOS33;
NET "rst" LOC ="K17" | IOSTANDARD = LVTTL | PULLDOWN ;
NET "inputfftlength<0>" LOC = "L13" | IOSTANDARD = LVTTL | PULLUP ;
NET " inputfftlength <1>" LOC = "L14" | IOSTANDARD = LVTTL | PULLUP ;

LVTTL: Low Voltage Transistor Transistor Logic.

6.3 DESIGN PROCEDURE

The experiment is carried out to validate the OFDMA system on vertex-5 FPGA board as briefed in the chapter-3 and also apply the FFT window positioning algorithm according to the delay mentioned by the ITU at a given instance of time. The flow of the synthesis in the FPGA board is shown in the Fig. 6.2.

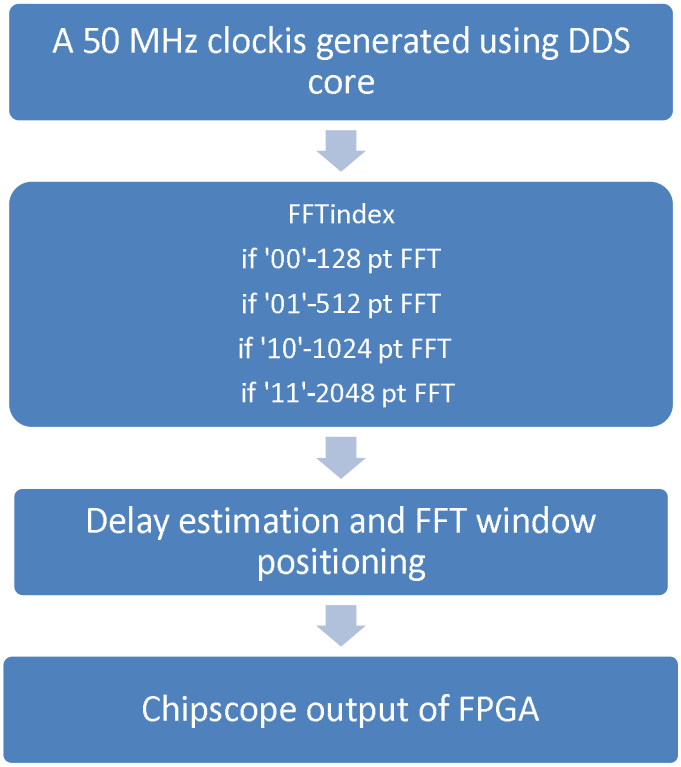

Fig.6.2 Flow of Synthesis of FFT Window positioned OFDMA

6.3.1 Test cases for verification

Once the FFT index is chosen and then the FFT window process should be delayed with respect to total delay produced by the various paths of symbols receiving at the receiver. This delay has been taken from delay profiles of ITU and that delay has been applied to the chipscope results of the OFDMA. Here different test cases have been considered like the receiver is at rest position, the receiver is pedestrian and receiver is moving with some velocity in the vehicle. So, all these three cases outputs have been verified and implemented on the Modelsim software and vertex FPGA hardware.

The ITU power delay profiles (PDP) defined by the recommendations of the ITU are well-established channel models for research of mobile communication systems. They specify channel conditions for various operating environments encountered in third-generation wireless systems. These systems operate in a 5 MHz bandwidth and are based on WCDMA principles. These are used to simulate the multipath fading channels [89], [90].

Table 6.2 ITU Channel Parameter Values

ITU-R	Delay(Tau) in µs	Power (P) in dB
Ped-A	[0 0.11 0.19 0.41]	[0 -9.7 -19.2 -22.8]
Ped-B	[0 0.2 0.8 1.2 2.3 3.7]	[0 -0.9 -4.9 -8 -7.8 -23.9]
Veh-A	[0 0.31 0.71 1.09 1.73 2.51]	[0 -1.0 -9.0 -10.0 -15.0 -20.0]
Veh-B	[0 0.3 8.9 12.9 17.1 20]	[-2.5 0 -12.8 -10.0 -25.2 -16.0]

6.4 RTL VIEW OF THE FFT PROCESSOR

The top view representation of a design is the Register Transfer Level (RTL) view which depicts the pin details and Input and Output of the system. The figure 5.3 and 5.4 represents the RTL view of the variable length FFT processor and its internal schematic. The system is synchronized with the clock signal and reset signal. The data transfer is taken place at the rising edge of the clock pulse.

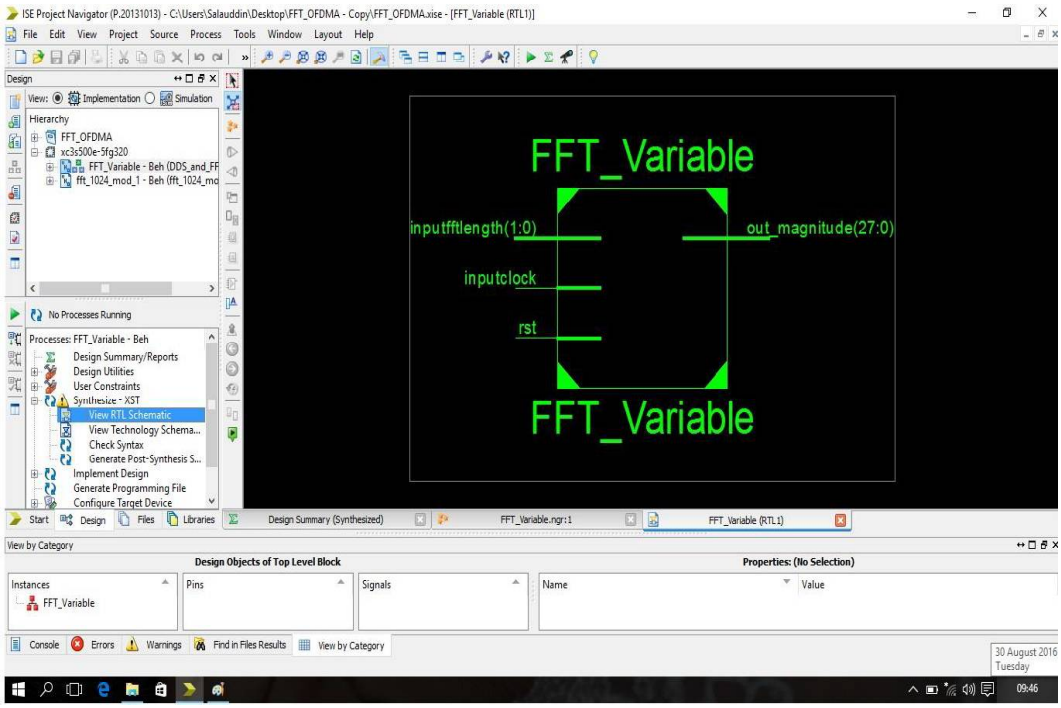

Fig.6.3. RTL view of Variable length FFT processor

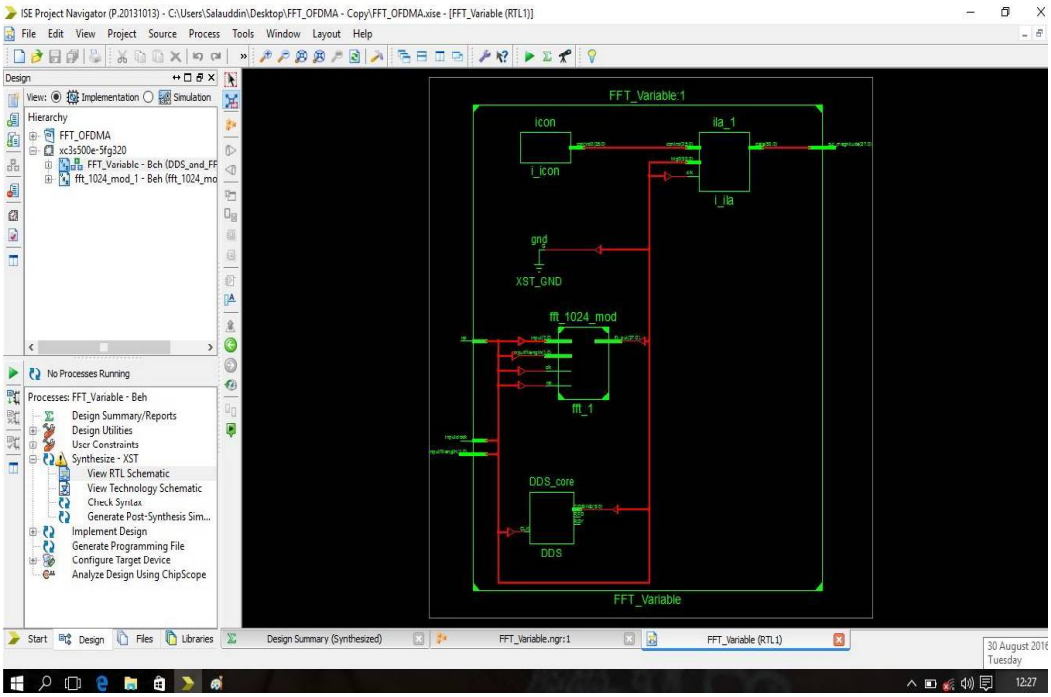

Fig.6.4. Internal Schematic of variable length FFT processor

In the Fig.6.3.FFT_variable is the block name, the inputs are declared in the input port, and inputfftlength, inputclock and rst are the inputs here. Inputfftlength [1:0] represents the index is of two bits i.e. 00, 01, 10 and 11 which selects the size of the FFT. Similarly out_magnitude[27:0] is the single output which is 28 bit long. Since long FFT's like 1024-pt FFT and 2048-pt FFT require large size registers for adder, multiplier, butterfly and twiddle factor calculations and storing. Similarly the Fig.6.4 shows the internal schematic of the FFT_variable block in which there are four separate blocks namely fft_1024_mod, DDS_core, ICON, ILA.

Fft_1024_mod is a block which computes the 128-pt FFT, 512-pt FFT, 1024-pt FFT, 2048-pt FFT depending on the inputfftlength which is of two bit length. DDS_core block is used to generate a 50MHz signal in which all the input points will be covered. Integrated Controller Core (ICON core) is the core which uses the JTAG Boundary Scan port to communicate to the host computer via a JTAG download cable. The ICON core provides a communications path between the JTAG Boundary Scan port of the target FPGA and up to 15 ILA, IBA/OPB, IBA/PLB, VIO, and/or ATC2 core. Integrated Logic Analyzer (ILA core) is a customizable logic

analyzer core that can be used to monitor any internal signal of your design. Since the ILA core is synchronous to the design being monitored, all design clock constraints that are applied to your design are also applied to the components inside the ILA core. The ILA core consists of three major components Trigger input and output logic, Data capture logic, Control and status logic [91], [92].

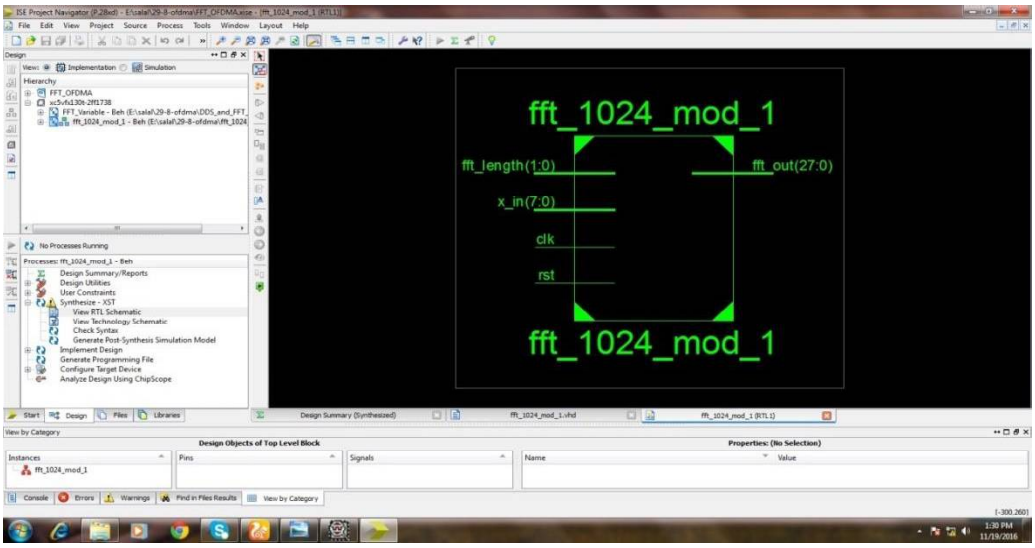

Fig.6.5. RTL View of 1024-pt-FFT

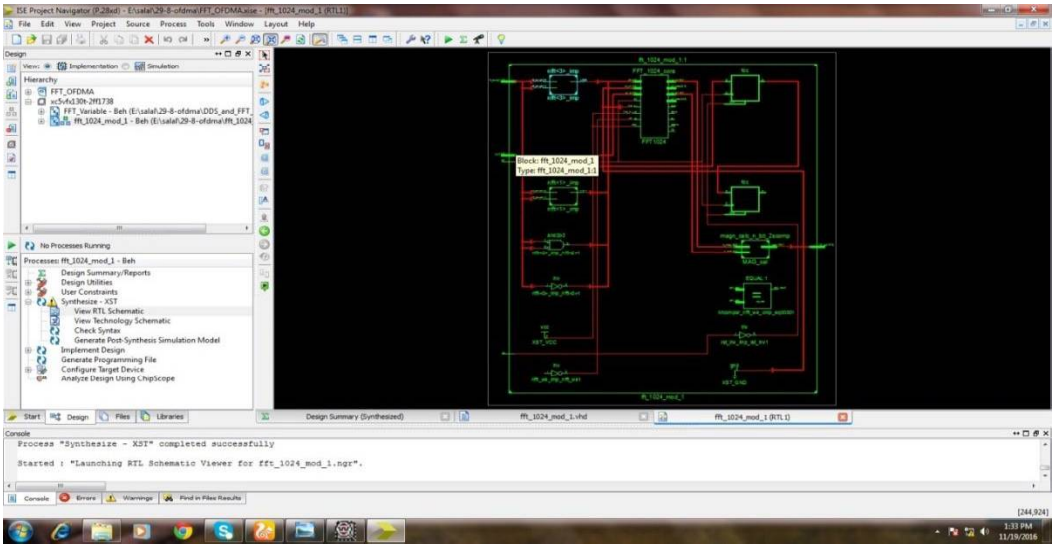

Fig.6.6. Internal Schematic of 1024-pt FFT

6.5 SIMULATION RESULTS

Modelsim10.1 b software is used for the simulation results which show the variable length FFT processor and the window positioning of the FFT process with respect to the delay produced by the interference. The screen shots of the same are attached in figure 6.7.1(a), (b), (c), (d) which represents the corresponding output for the corresponding delays. The functional simulation depends on the test inputs in design. Clock and reset are used for the synchronization. The FFT functional simulation and the positioned window of FFT simulation guarantees the successful completion of variable FFT with respect to delay and the FPGA synthesis guarantees the hardware feasibility of the simulated chips to fabrication foundries.

6.5.1 Test cases of functional simulation

I) Ideal Test Case: In this Test case the delay is considered as zero and depending on the FFT index the FFT point is chosen as shown and discussed in the figure 6.5.1(a). The time taken to calculate the same are given in the table 6.3

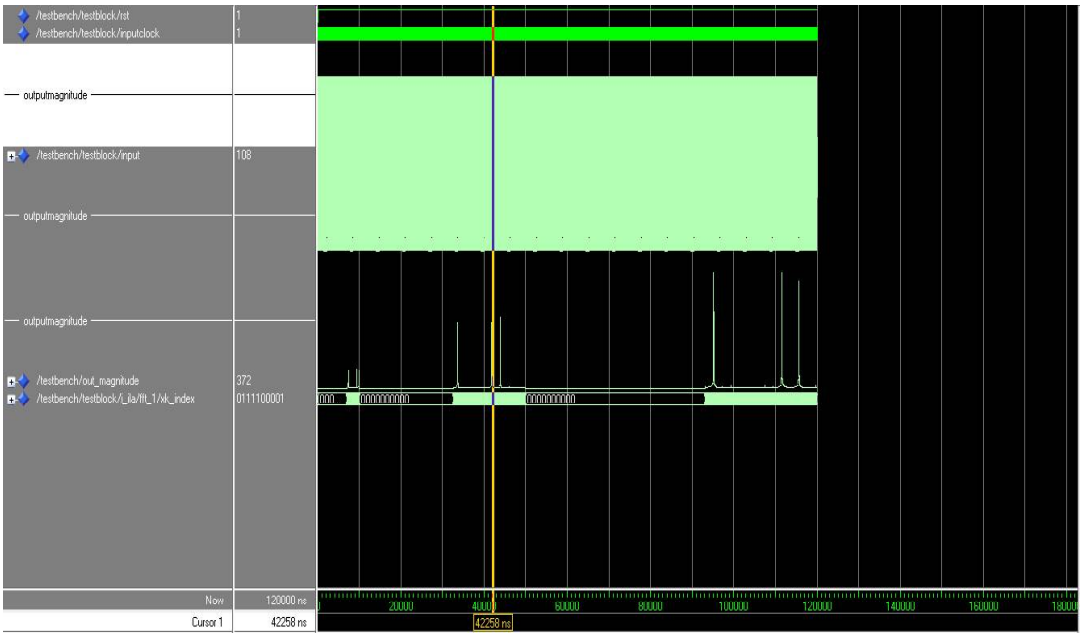

Fig.6.7.1 (a) Simulation of Variable length FFT processor with delay=0 µs

Table 6.3 Timing Calculation of Variable FFT when delay= 0 µs.

Delay =0 µs				
FFT Index	FFT Length	Peak started at	Peak ended	Total time
00	128-pt FFT	0	7.37 µs	7.370µs
01	512-pt FFT	9.945 µs	33.653 µs	23.708 µs
10	1024-pt FFT	43.909 µs	95.166 µs	51.257 µs
11	2048-pt FFT	111.56 µs	216.344µs	104.78 µs

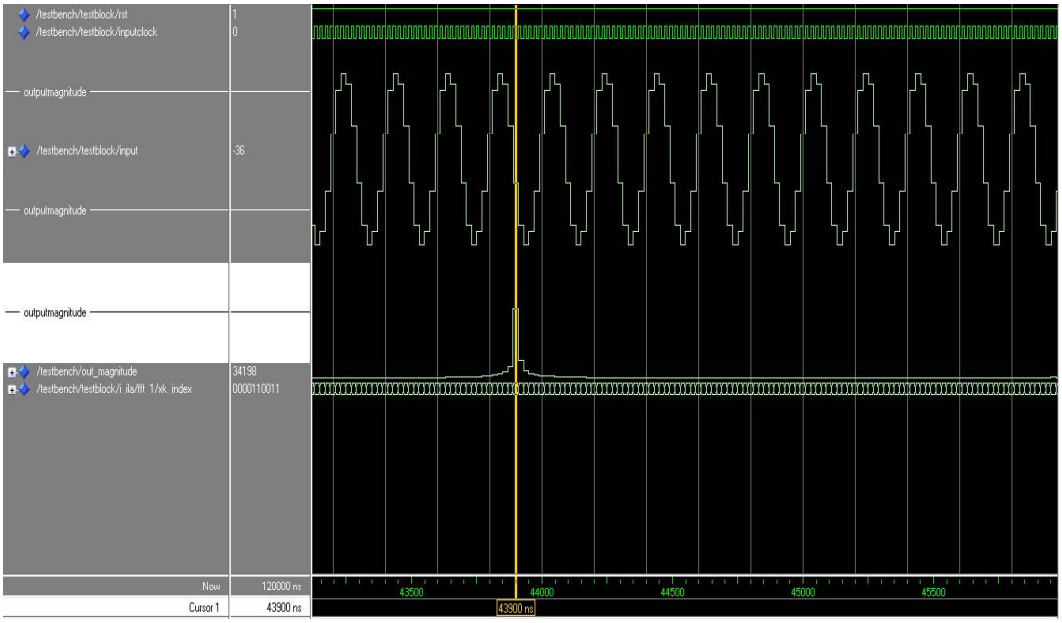

Fig.6.7.1 (b) Simulation result with index '10' and peak starting at 43.09 µs when delay=0.

The simulation result of variable length FFT processor with index '10' and delay=0 is shown as an example and the peak is at 43.09 µs. similarly other two cases have been considered with delay =0.41 µs for pedestrian and delay= 2.51 µs for vehicular on the basis of the delays produced by the ITU at a particular instance of time as shown in the Table 6.2.

II) Pedestrian Test Case: Delay=0.41 µs

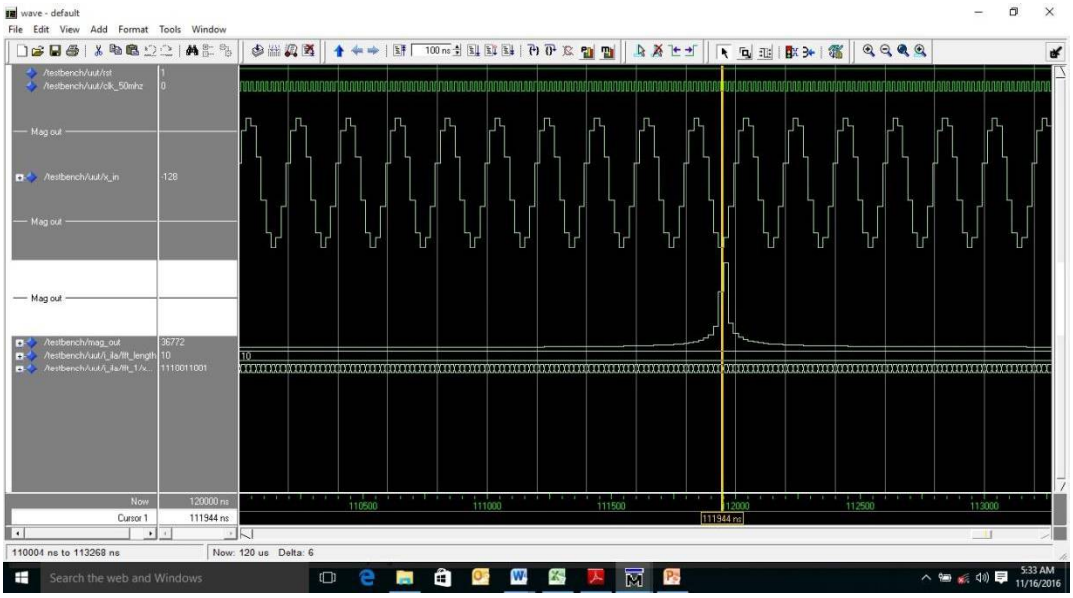

Fig. 6.7.1(c) Simulation result with index '11' and peak starting at 111.944 µs when delay=0.41 µs

Table 6.4 Timing Calculation of Variable FFT when delay= 0.41 µs.

Delay =0.41 µs				
FFT Index	FFT Length	Peak started at	Peak ended	Total time
00	128-pt FFT	0	7.78 µs	7.78µs
01	512-pt FFT	10.355 µs	34.065 µs	23.710 µs
10	1024-pt FFT	44.323 µs	95.576 µs	51.253 µs
11	2048-pt FFT	111.944 µs	216.754µs	104.81 µs

III) Vehicular Test Case: Delay=2.51 µs

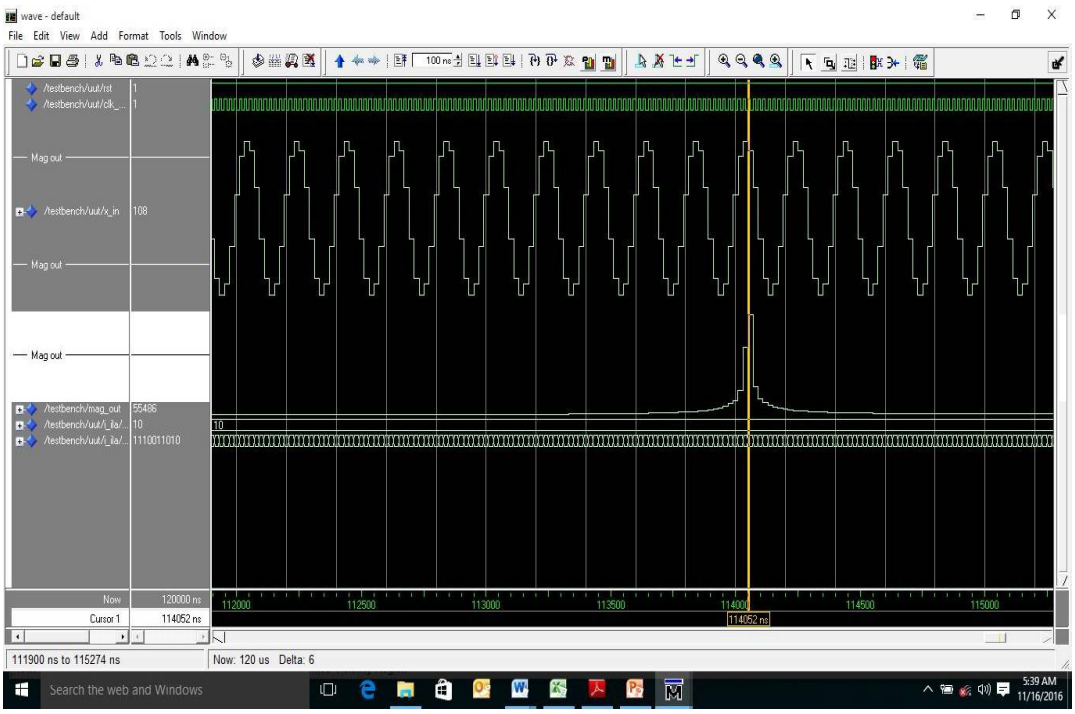

Fig. 6.7.1(d) Simulation result with index '11' and peak starting at 114.052 µs when delay=2.51 µs

Table 6.5 Timing Calculation of Variable FFT when delay= 2.51 µs.

Delay =2.51 µs				
FFT Index	FFT Length	Peak started at	Peak ended	Total time
00	128-pt FFT	0	9.88 µs	9.88 µs
01	512-pt FFT	12.455 µs	36.173 µs	23.718 µs
10	1024-pt FFT	46.419 µs	97.676 µs	51.257 µs
11	2048-pt FFT	114.052 µs	218.854µs	104.802 µs

The simulation results show that the calculation time for 128-pt FFT is 9.88 µs, 512-pt FFT is 23.718 µs, 1024-t FFT is 51.257 µs and 2048-pt FFT is 104.802 µs and this equal for all the three considered cases i.e. ideal, pedestrian and vehicular but in the three cases the position of the FFT window has been shifted with respect to delay i.e pedestrian 0.41 µs and vehicular 2.51 µs. Hence the objective of shifting the position of the FFT window

is achieved on simulation and the next section describes the same on the hardware i.e the synthesis results.

6.6 SYNTHESIS RESULTS

The synthesis has been carried out on the Xilinx Vertex-5 XC5VLX130T FPGA board with the same test cases used for the simulation of the system i.e. delay=0, delay= 0.41 µs and the delay = 2.51 µs. here also the analysis has been carried out between the data VS time . The same has been shown in the Fig. 6.6.1 (a), (b) and (c).

6.6.1 SYNTHESIS TEST CASES

I) Ideal Test Case:

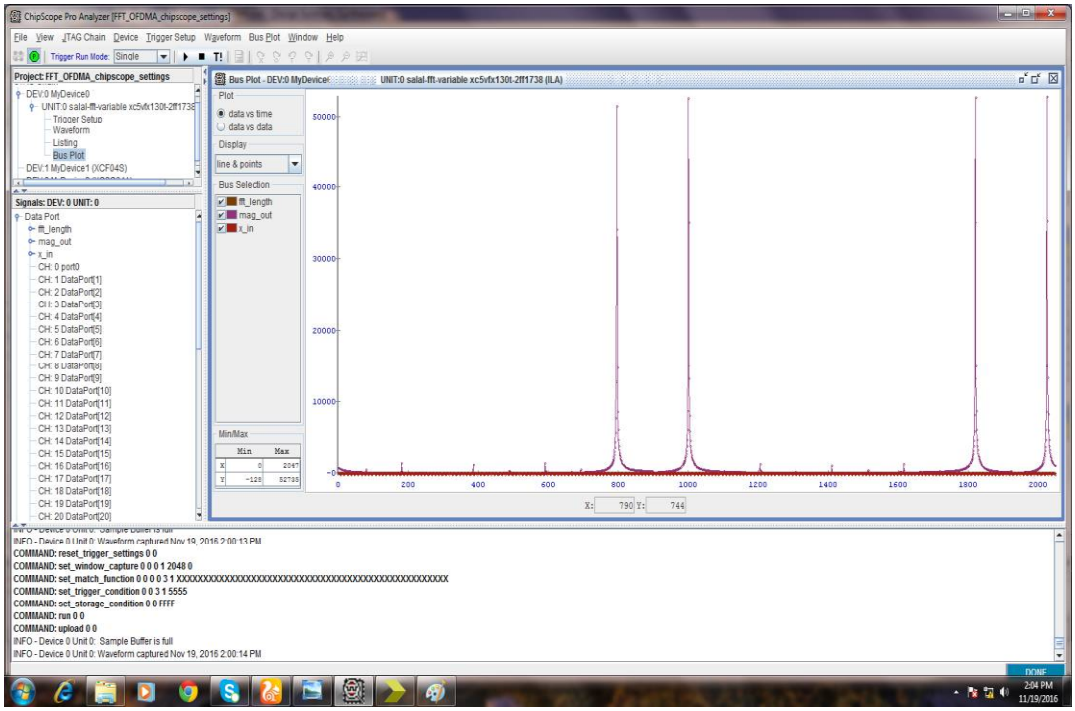

Fig.6.8.1. (a) Synthesis of Variable length FFT processor with delay=0µs

Table 6.6 Hardware Timing Calculation of Variable FFT when delay= 0.

Delay =0				
FFT Index	FFT Length	Peak started at	Peak ended	Total time
00	128-pt FFT	0	7.90 µs	7.90µs
01	512-pt FFT	10.575 µs	35.216 µs	25.208 µs
10	1024-pt FFT	44.539 µs	98.396 µs	53.857 µs
11	2048-pt FFT	113.19 µs	220.57 µs	107.38 µs

II) Pedestrian Test Case: Delay=0.41 µs

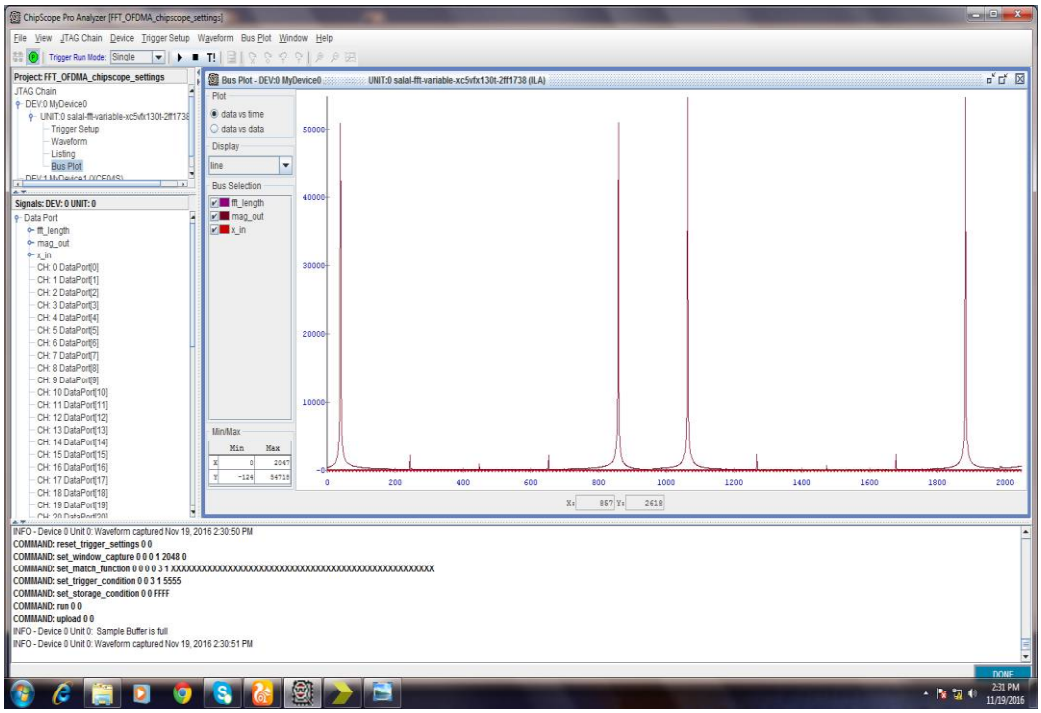

Fig.6.8.1. (b) Synthesis of Variable length FFT processor with delay=0.41 µs

Table 6.7 Hardware Timing Calculation of Variable FFT when delay= 0.41 µs.

Delay =0.41 µs				
FFT Index	FFT Length	Peak started at	Peak ended	Total time
00	128-pt FFT	0	8.31 µs	8.31µs
01	512-pt FFT	10.985 µs	36.195 µs	25.212 µs
10	1024-pt FFT	44.949 µs	98.839 µs	53.890 µs
11	2048-pt FFT	113.60 µs	220.98 µs	107.38 µs

III) Vehicular Test Case: Delay=2.51 µs

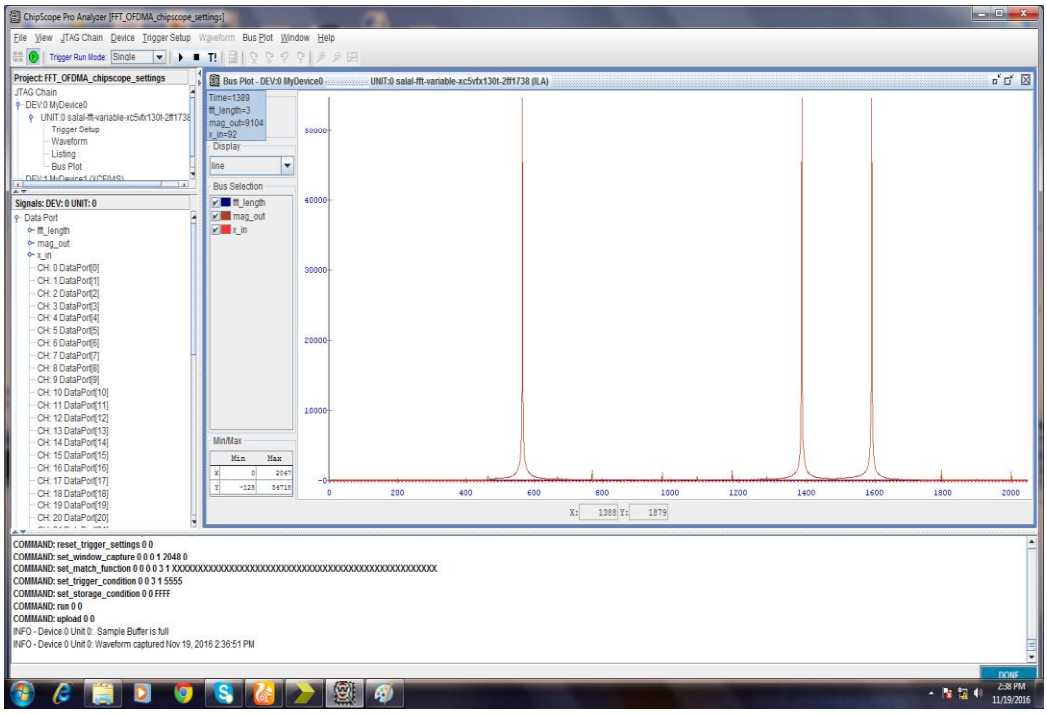

Fig.6.8.1. (c) Synthesis of Variable length FFT processor with delay=2.51 µs

Table 6.8 Hardware Timing Calculation of Variable FFT when delay= 2.51 µs.

Delay =2.51 µs				
FFT Index	FFT Length	Peak started at	Peak ended	Total time
00	128-pt FFT	0	10.41 µs	10.41µs
01	512-pt FFT	13.885 µs	39.330 µs	25.445 µs
10	1024-pt FFT	47.049 µs	98.639 µs	53.690 µs
11	2048-pt FFT	115.70 µs	221.18 µs	107.69 µs

Fig. 6.8.1 (a), 6.8.1(b) and 6.8.1(c) shows the synthesis results of the window positioned FFT in the presence of interference. The time taken by the FPGA to compute 128-pt FFT is 10.41 µs, 512-pt FFT is 25.445 µs, 1024-pt FFT is 53.690 µs and 20148-pt FFT is 107.69 µs. When compared with the simulation results the hardware implementation took more time to compute the same but the objective of positioning the FFT window in the presence of interference has been achieved.

6.7 H ARDWARE IMPLEMENTATION OF OFDMA

6.7.1. Simulation of Symbols going to IFFT Input

In the implementation of OFDMA 64-symbols have been transmitted with 8-bit parallel data as the input of IFFT at an instance of time. 8-point FFT is the main block of the implementation of 2D-FFT implementation of the OFDMA. Simulation results of the symbols going at the input of IFFT is shown in the Fig.6.9.1 16-bit registers have been used with 10-bit fractional part is implemented for the same. The same input can be divided by 1024 to get the MATLAB obtained results.

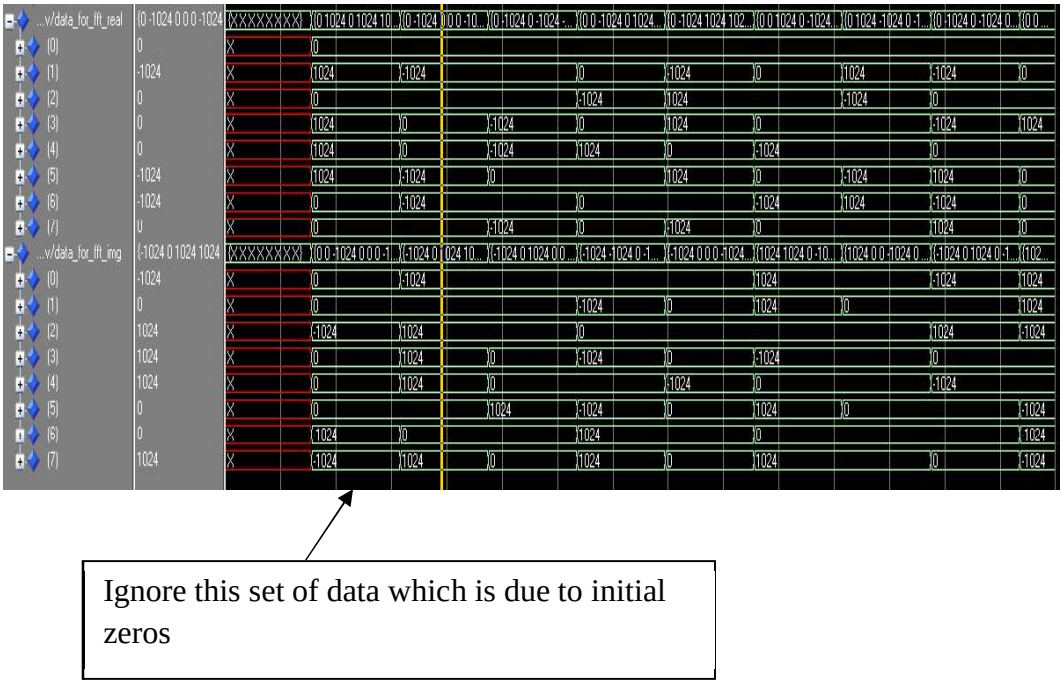

Fig.6.9.1 Symbols going to IFFT for OFDMA implementation

6.7.2 Symbols of IFFT output

Simulation results of the symbols coming from the output of IFFT is shown in the Fig.6.9.1 16-bit registers have been used with 10-bit fractional part is implemented for the same. The same output can be divided by 1024 to get the MATLAB obtained results of the IFFT.

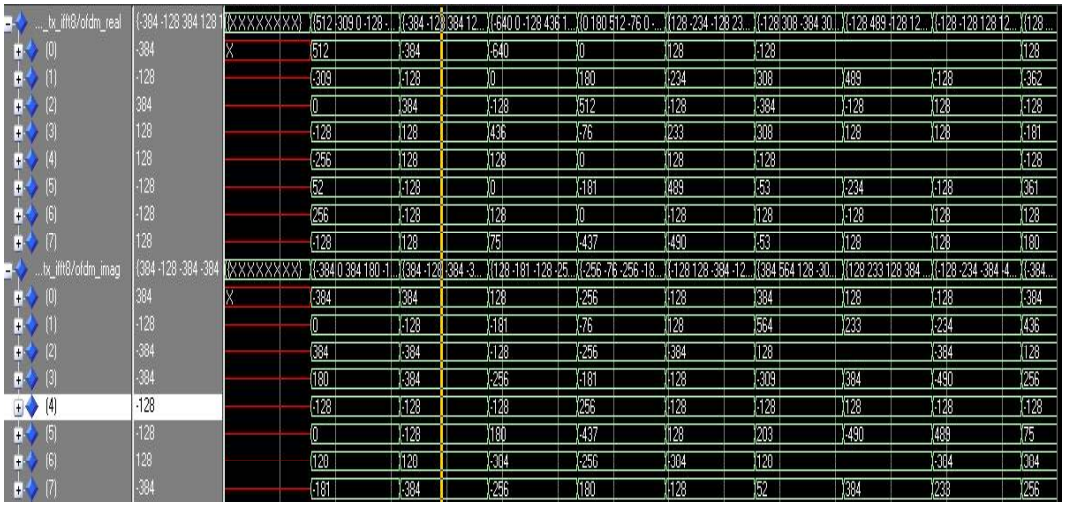

Fig.6.9.2. Symbols coming from IFFT output for OFDMA implementation

6.7.3 Simulation of window positioned OFDMA

The simulation of window positioned OFDMA is shown in the Fig.6.9.2. in which transmitted signal and the received signal has been shown and received signal output has been delayed with respect to the delay then the FFT will be implemented. The start and end of the arrow in the Fig.6.9.2. is the transmitted signal and the delayed received signal processing in OFDMA.

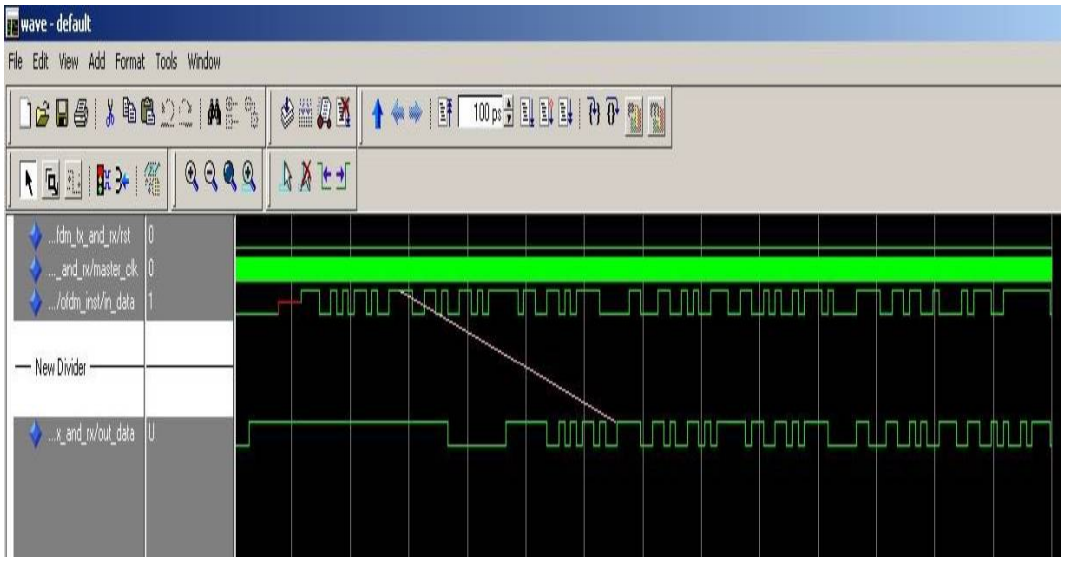

Fig.6.9.3. Simulation of window positioned OFDMA

6.7.4 Synthesis result of window positioned OFDMA

Fig.6.9.4 shows the result of the FFT window positioned OFDMA on the hardware. The transmitted signal and the received signal are shown in the figure. The received signal output processing has been delayed by 1.6μs ensuring that all the symbols have been received at the receiver thus reducing the bit error rate.

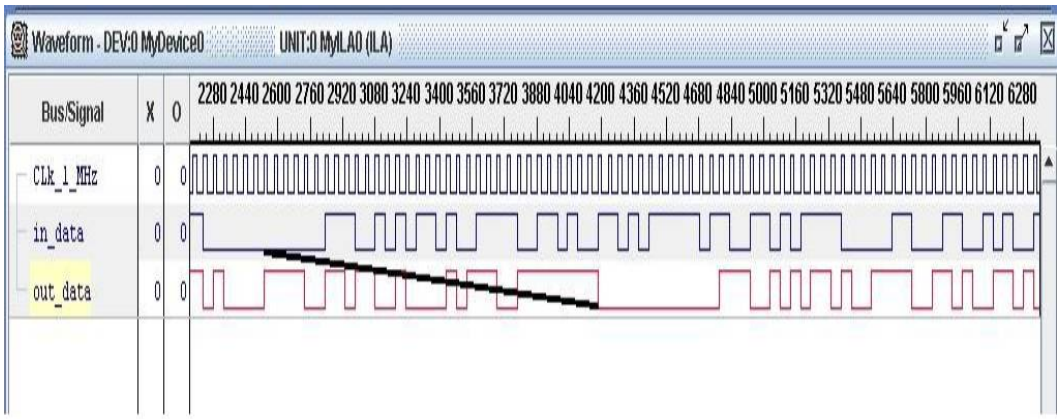

Fig.6.9.4. Synthesis result of window positioned OFDMA

6.8 REPORT SUMMARY AND DEVICE UTILIZATION

The detailed description of the Synthesis Options Summary, Hardware Description Language (HDL) Synthesis Report, Advanced HDL Synthesis Report, Device utilization summary, Timing Report has been shown in this following section.

6.8.1 Synthesis options summary

Table 6.9 Summary of Synthesis options

Synthesis Options Summary
Source Parameters
Input File Name : "FFT_Variable.prj"
Input Format : mixed
Ignore Synthesis Constraint File : NO
Target Parameters
Output File Name : "FFT_Variable"
Output Format : NGC
Target Device : xc5vfx130t-2-ff1738
Source Options
Top Module Name : FFT_Variable
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Mux Style : Auto
Decoder Extraction : YES
Priority Encoder Extraction : Yes
Shift Register Extraction : YES

Logical Shifter Extraction : YES
XOR Collapsing : YES
ROM Style : Auto
Mux Extraction : Yes
Resource Sharing : YES
Asynchronous To Synchronous : NO
Use DSP Block : Auto
Automatic Register Balancing : No
Target Options
LUT Combining : Off
Reduce Control Sets : Off
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 32
Register Duplication : YES
Slice Packing : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES
General Options
Optimization Goal : Speed

Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Verilog 2001 : YES
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

6.8.2 HDL Synthesis report

Table 6.10 HDL Synthesis Report

# ROMs	16
64x14-bit ROM	16
# Multipliers	162
14x14-bit multiplier	162
# Adders/Subtractors	315
14-bit adder	300
28-bit adder	1
6-bit adder	14
# Counters	2
3-bit up counter	1
6-bit down counter	1
# Registers	1088
14-bit register	1024
6-bit register	64
# Toggle Registers	2
T flip-flop	2
# Multiplexers	36
14-bit 64-to-1 multiplexer	2
6-bit 64-to-1 multiplexer	8
# Xors	400
1-bit xor2	400

6.8.3 Device utilization summary

Table 6.11 Device utilization summary

Device utilization summary
Selected Device : 5vfx130tff1738-2
Slice Logic Utilization
Number of Slice Registers : 5700 out of 81920 6%
Number of Slice LUTs: 10865 out of 81920 13%
Number used as Logic: 10865 out of 81920 13%
Slice Logic Distribution
Number of LUT Flip Flop pairs used: 14267
Number with an unused Flip Flop: 8567 out of 14267 60%
Number with an unused LUT: 3402 out of 14267 23%
Number of fully used LUT-FF pairs: 2298 out of 14267 16%
Number of unique control sets: 37
IO Utilization
Number of IOs: 32
Number of bonded IOBs: 32 out of 840 3%
Specific Feature Utilization
Number of BUFG/BUFGCTRLs: 4 out of 32 12%
Number of DSP48Es: 134 out of 320 41%

6.8.4 Timing summary

Speed Grade: -2

- Minimum period: 33.459ns
- Minimum input arrival time before clock: No path found
- Maximum output required time after clock: 9.225ns
- Maximum combinational path delay: 6.732ns

6.9 SIMULATION OF OFDMA ON MATLAB

The overall OFDMA system was simulated on the MATLAB for the both conventional OFDMA and the FFT window positioning of OFDMA in the presence of interference. The carrier frequency used here is set to 3GHz and the channel bandwidth is chosen to be 20 MHz for the simulation of the overall system. The other parameters like spacing between the carriers, size of the FFT/IFFT performed and sampling rate are chosen accordingly. The digital modulation scheme used is Quadrature Amplitude modulation and the modulation order remains to be 64, since for high data rate applications like DVB-H and DVB-T 64-QAM is preferred over the other digital modulation schemes. The parameters used in the simulation are listed below.

Table 6.12 Parameters of OFDMA simulation

Parameter	**Value**
Carrier frequency	3 GHz
Channel Bandwidth	20 MHz
Spacing between subcarriers	15 KHz
Number of Occupied subcarriers	1200
IFFT/FFT size	2048

Sampling rate	30.72 MHz
Modulation Scheme	QAM
Modulation order	64
CP length	144 samples
Maximum Doppler frequency	333.33Hz

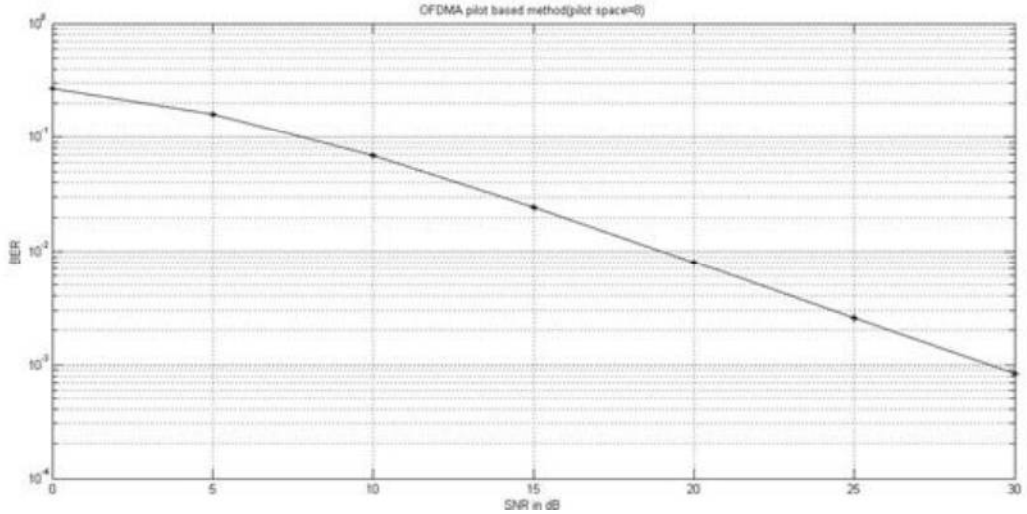

Fig 6.10 BER VS SNR of Conventional OFDMA system in MATLAB

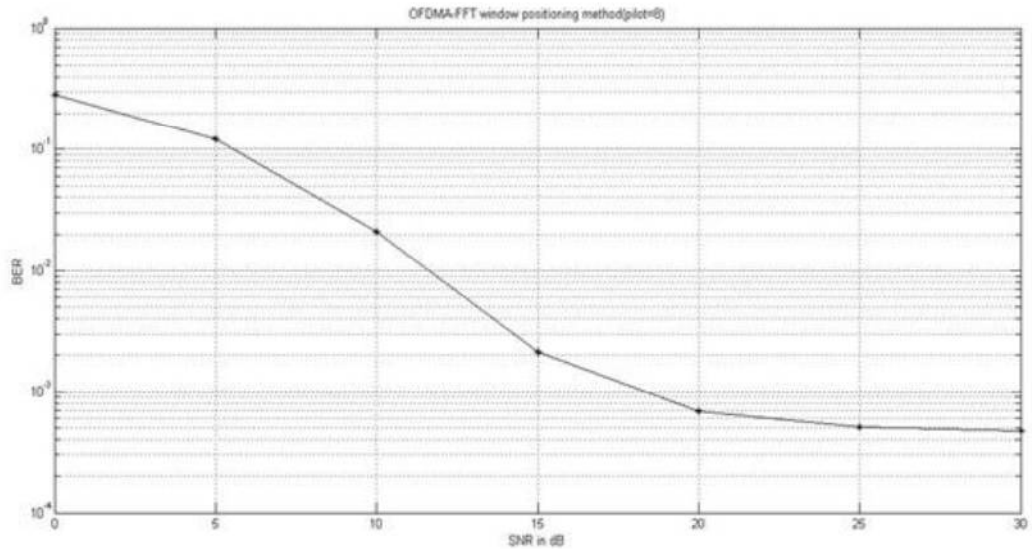

Fig 6.11 BER VS SNR of FFT Window positioned OFDMA

In the Fig 6.10 and Fig 6.11 it can be observed that the simulation was carried out for the conventional OFDMA and the window positioned FFT- OFDMA. The BER for the FFT window positioned OFDMA is derived from the delay given to the FFT operation window ensuring that all the symbols have been arrived at the receiver , then start the processing of the FFT. The fractional delay has been provided by the farrow filters and hence it has been observed that the BER for conventional OFDMA is 0.0080 at 20dB and 0.00060 for FFT window positioned OFDMA. Hence an SNR improvement of 7.5% has been observed for the same.

6.10 SUMMARY

The section 6.2 gives the description of the synthesis tool used i.e. Xilinx vertex-5 FPGA and flow of synthesis has been shown in section 6.3 followed by the section 6.4 gives the RTL views of the OFDMA system designed by using 2D-FFT algorithm. This gives the information about the overall block diagram of the system FFT-Variable and its internal schematic block diagram and also RTL view of 1024-pt FFT is also shown in the same. Section 6.5 shows the simulation results on the Modelsim 10.2 software. In which all the comparisons of timing of 128-pt FFT, 512-pt FFT, 1024-pt FFT and 2048-pt FFT has been shown. Similarly the synthesis results are shown in the section 6.6. which shows the comparisons of timing of 128-pt FFT, 512-pt FFT, 1024-pt FFT and 2048-pt FFT on hardware. It has been observed that the hardware implementation takes more time to calculate the same. The hardware implementation of OFDMA is shown in the section 6.7 in which both simulation and synthesis outputs are discussed. Section 6.8 gives the detailed description of device utilization and timing summary report and in the section 6.9 the results of simulation of conventional OFDMA and FFT window positioned OFDMA on MATLAB.