Name: **Enrolment No:**	

UPES

End Semester Examination, December 2023

Program Name: Electronics & Communication Engineering **Semester : V**

Course Name: IC Design and Fabrication **Time : 3 hrs**

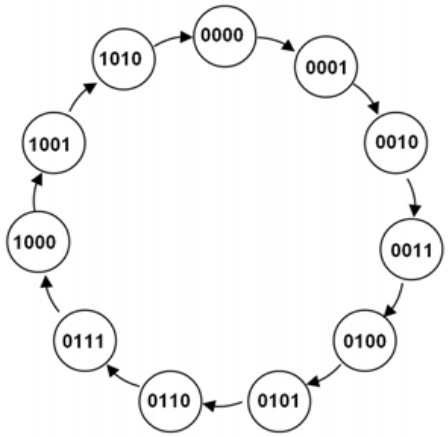
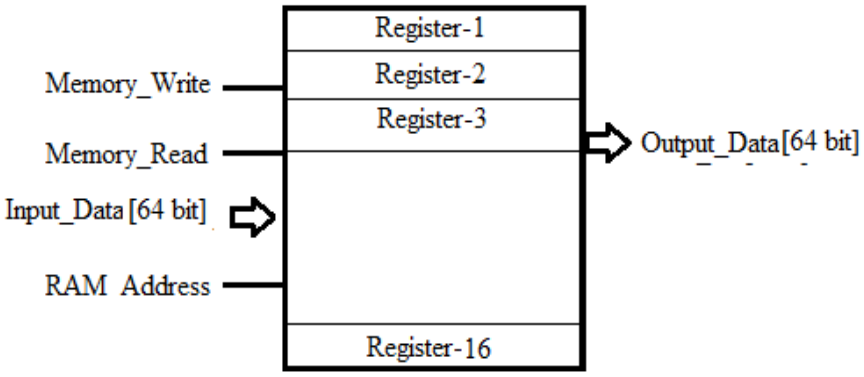
Course Code: ECEG-3081P **Max. Marks: 100**

Nos. of page(s): 2

Instructions: Assume any data in the design, if required.

SECTION A
(5Q x 4M = 20 Marks)

S. No.		Marks	CO
Q.1	Which generations of integrated circuits are distinct? Discuss with examples	**5**	**CO1**
Q.2	Design the 11-bit even/odd parity generator using any HDL with complete functionality.	**5**	**CO2**
Q.3	Design the negative edge triggered synchronous 'D' flip flop using flip flop.	**5**	**CO3**
Q.4	Detail the concept of ion implantation in IC fabrication.	**5**	**CO4**
	SECTION B **(4Q x 10M = 40 Marks)**		
Q.5	Draw the structure of CPLD (Max Altera 7000) and explain the functionality. Compare the CPLD with FPGA. ***OR*** Design the full subtractor chip in all styles of modeling.	**10**	**CO4**
Q.7	Design the hardware chip for the functionality of (8x3) encoder using all styles of modeling	**10**	**CO2**
Q.8	Discuss in detail the fabrication methodology and steps of npn- BJT	**10**	**CO3**
Q.9	Compare ASIC and FPGA technologies based on their design flow, functionality, and types.	**10**	**CO3**
	SECTION-C **(2Q x 20M = 40 Marks)** **Attempt any *two* of the followings**		
Q.10	(a) Design the IC of 16-bit shifter using behavior model that perform the following operation *Shift left by 1 bit* *Shift right by 1 bit* *Rotate left by 1 bit* *Rotate right by 1 bit*	**10+10**	**CO1**

Q.11	(a) Compare the concept of Mealy and Morre FSM design. Develop the VHDL code for counter shown below for up/down operation sequentially.  Fig.1 Counter **(b)** Consider a memory system (16 x 64) which has 8 Registers as shown in Fig.2. The input data CAF1H is written and read at different time intervals with 0.8 ms delay in all registers respectively. Suggest the algorithm for the complete RAM locations to store the data from input port and send to output port. Calculate the time required to perform the data storage in all registers. Also develop the code in VHDL, or any other language. .  Fig.2 RAM structure	**10+10**	**CO2**
Q.12	(a) Detail the concept of optical lithography in IC fabrication process. (b) Detail the fabrication processing steps and complete methodology of twin tub process for CMOS fabrication.	**5+15**	**CO3**