Name: **Enrolment No:**	UPES UNIVERSITY OF TOMORROW

UPES

End Semester Examination, December 2023

Program Name: Electronics & Communication Engineering **Semester : V**

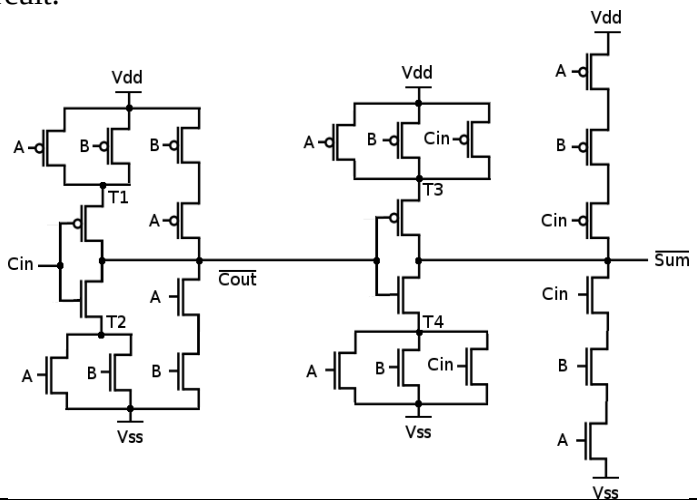
Course Name: VLSI Design **Time : 3 hrs**

Course Code: ECEG-3049 **Max. Marks: 100**

Nos. of page(s): 2

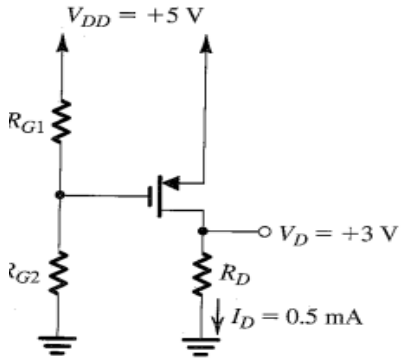
Instructions: Assume any data in the design, if required

SECTION A (5Q x 4M=20Marks)

S. No.		Marks	CO
Q.1	Explain the concept of channel length modulation in N-MOSFET.	**5**	**CO1**
Q.2	Discuss the concept of ratio less dynamic logic using pass transistor.	**5**	**CO3**
Q.3	How NMOS can be used as an inverter. Explain with circuit and characteristics.	**5**	**CO3**
Q.4	What is the need for low power CMOS circuit design. Justify the output of the following circuit. 	**5**	**CO4**

SECTION-B (4Q x 10M= 40 Marks)

Q.5	Draw the stick diagram and layout diagram of the 2- input XOR and NAND gate using NMOS and CMOS.	**10**	**CO4**
Q.7	Design the circuit described using the function given below using CMOS. $Y_1 = \overline{A(B+C)(D+E)}$ $Y_2 = \overline{(A+B+C)(D+E)}$ Also find the equivalent CMOS inverter circuit for simultaneous switching of all inputs assuming that $(W/L)_p = 5$ for all PMOS transistors and $(W/L)_n = 2$ for all NMOS transistors. **OR** Implement all the following logic (*AND, NAND, NOR, OR XOR*) gates using NMOS and CMOS.	**10**	**CO2**

Q.8	Detail the following with respect to MOSFET circuits. (a) Speed of operation (b) Noise Margin in CMOS (c) Power delay product (d) Propagation delay (e) $\mu = r_d \times g_m$.	**10**	**CO3**
Q.9	Write the detailed steps in CMOS fabrication using P-well process.	**10**	**CO1**
SECTION-C (2Q x 20M = 40 Marks) **Attempt any *two* of the followings**			
Q.10	(a) Draw the voltage transfer curve for the CMOS inverter and derive the mathematical expression to estimate the value of V_{OH}, V_{OL}, V_{IH} and V_{IL} for NMOS inverter circuit and detail the functionality. (b) Sketch the PMOS and NMOS transistor large signal model.	**15+5**	**CO3**
Q.11	**(a)** Determine the mathematical expression for the drain current for the entirety of the N-MOSFET's functioning in each region. **(b)** Design the circuit shown in Fig. to operate the transistor in saturation region. I_D=0.5 mA, V_D = + 3V, K'$_p$.(W/L) = 1 mA/V^2, V_t = -1 V  Assume the channel length modulation is zero. Calculate the value of R_D maximum to maintain the enhancement type P-MOSFET in saturation.	**10+10**	**CO2**
Q.12	Compare the all PLD technology and realize the following functions using all technology at gate level and N-MOSFT level. $F_1 = wxyz + \bar{w}xyz + \bar{w}xyz + wx\bar{y}\bar{z}$ $F_2 = wxyz + \bar{w}xyz + w\bar{x}yz + w\bar{x}y\bar{z}$ $F_3 = wxyz + +\bar{w}x\bar{y}z$ $F_4 = w\bar{x}y\bar{z} + \bar{w}xyz + \bar{w}xy\bar{z} + w\bar{x}yz$	**20**	**CO4**