Name: **Enrolment No:**	

UPES

End Semester Examination, December 2023

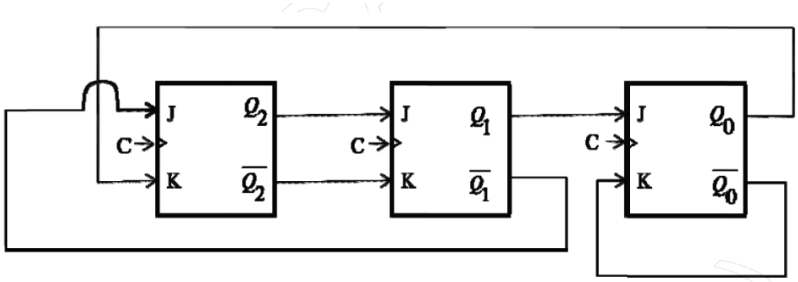
Course: Computer System Architecture **Semester: III**

Program: B.Tech-CSE **Time : 03 hrs.**

Course Code: CSEG2004 **Max. Marks: 100**

SECTION A
(5Qx4M=20Marks)

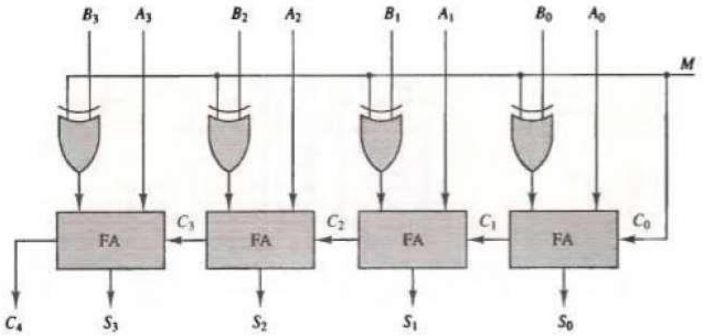
S. No.		Marks	CO
Q 1	A memory system consists of cache and main memory. If it takes 1 cycle to complete a cache hit and 100 cycle to complete a cache miss. What is the average memory access time if the hit rate in the cache is 97%.	**5**	**CO4**
Q 2	State differences between static and dynamic RAM.	**5**	**CO1**
Q 3	Explain the role of control unit in instruction interpretation and instruction execution.	**5**	**CO2**
Q 4	Discuss various registers used in the basic computer.	**5**	**CO3**
Q 5	Explain the concept of sequential circuit with the help of example.	**5**	**CO2**
	SECTION B **(4Qx10M= 40 Marks)**		
Q 6	What are the different memory reference instructions used in the basic computers. Explain each with an assembly code.	**10**	**CO2**
Q 7	(a) What is content addressable memory? (b) A digital computer has a memory unit of (64K X 16) and a cache memory of 1K words. The cache uses direct mapping with a block size of 4 words. • How many bits are there in the tag, index, block, and word fields of the address format? • How many bits are there in each word of cache, and how are they divided into functions? Include a valid bit. • How many blocks can the cache accommodate?	**10**	**CO3**

<table>
<tr><td>Q 8</td><td>Discuss the stack organization of CPU in basic computer for memory and registers.
OR
What is superscalar processing. Explain it with an example.</td><td>10</td><td>CO2, CO3</td></tr>
<tr><td>Q 9</td><td> 

The above sequential circuit is built using JK flip-flops is initialized with Q2Q1Q0 = 000. Find the state sequence for this circuit for the next 3 clock cycle.</td><td>10</td><td>CO1</td></tr>
<tr><td colspan="4">SECTION-C
(2Qx20M=40 Marks)</td></tr>
<tr><td>Q 10</td><td>Compare and contrast direct-mapped, set-associative, and fully associative cache memory mapping techniques. Discuss the strengths and weaknesses of each approach and provide examples of when it's advantageous to use one technique over the others. Explain the key design considerations associated with implementing each mapping technique in computer systems.</td><td>20</td><td>CO4</td></tr>
<tr><td>Q 11</td><td>(a) Write short notes on
• Memory Address Register (MAR)
• Memory Data Register (MDR)

(b) The adder-subtractor circuit shown below has the following values for input mode M and data inputs A and B. In each case, determine the values of the outputs: S3, S2, S1, S0, and C4.

<table>
<tr><td></td><td>M</td><td>A</td><td>B</td></tr>
<tr><td>a</td><td>0</td><td>0111</td><td>0110</td></tr>
<tr><td>b</td><td>0</td><td>1000</td><td>1001</td></tr>
<tr><td>c</td><td>1</td><td>1100</td><td>1000</td></tr>
<tr><td>d</td><td>1</td><td>0101</td><td>1010</td></tr>
<tr><td>e</td><td>1</td><td>0000</td><td>0001</td></tr>
</table>
</td><td>20</td><td>CO1</td></tr>
</table>



OR

Write a program to evaluate the arithmetic statement:

$$X = \frac{A - B + C * (D * E - F)}{G + H * K}$$

(a) Using a general register computer with three address instructions.
(b) Using a general register computer with two address instructions.
(c) Using an accumulator type computer with one address instructions.
(d) Using a stack organized computer with zero-address operation instructions.