COMPARATIVE STUDY OF VARIOUS SOLAR PANEL MANUFACTURING TECHNOLOGIES

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Master of Technology

(Energy Systems)

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CERTIFICATE

This is to certify that the work contained in this thesis titled **"COMPARATIVE STUDY OF VARIOUS SOLAR PANEL MANUFACTURING TECHNOLOGIES"** has been carried out by Sanjay Kumar Swami under my supervision and has not been submitted elsewhere for a degree.

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Abstract

Concerns over global climate change, local air pollution, and resource scarcity make photovoltaic (PV) an increasingly attractive energy supply technology. But current PV technology, which is based primarily on silicon wafers, is more expensive than conventional power generation and, despite rapid growth, still only competes in niche and subsidized applications. As a result, research is progressing on a wide array of alternative materials in an effort to improve performance and reduce costs. How do the costs and performance of these other PV technologies compare to silicon wafers? In this report, evaluate the technical characteristics of "thin film" alternatives to silicon wafers. Assess their future potential in the context of a photovoltaic market that increasingly favors crystalline silicon. It finds that, for commercially available modules, silicon wafers are both cheaper and more efficient. However, the differences in performance between silicon wafers and thin- films are diminishing. Materials costs are lower for the thin film technologies, although obstacles to commercialization exist for each. Finally, suggests that the variety of materials upon which thin films are based engenders them with unique characteristics such that in the future they may compete not only on cost but by enabling a more diverse set of applications than exists today.

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CHAPTER 1

Introduction

The long and increasing dominance of crystalline silicon in the photovoltaic (PV) market is perhaps surprising given the wide variety of materials capable of producing the photovoltaic effect. PV based on silicon wafers has captured more than 85% market share because it is more reliable, and generally more efficient than competing technologies. Silicon wafers have benefited from dramatically cheaper raw materials and economies of scale.

Yet, research continues on developing a diverse set of alternative photovoltaic technologies such as thin film technology, dye sensitized solar cell and organic solar cell.

In this report, efforts are done, to do comparative study of alternatives to the silicon wafer technology, and to access their future potential in the context of a photovoltaic market (that currently increasingly favors crystalline silicon). It is being found that the attractiveness of these alternatives is based mainly on their future potential to displace crystal wafers, rather than near-term expectations about their competitiveness.

The most important attributes of the "thin films" are lower materials costs, and characteristics such as flexibility. The potential, advantages and disadvantage each technology.

In thin film technologies different type of material used such as amorphous silicon (a-Si), copper Indium gallium diselenide (CIGS), cadmium telluride (CdTe). Efficiency of thin film technology in comparison of crystalline is less.

Dye-sensitized solar cell (DSSC) and organic solar cell which are new in the market, cheaper but lees efficient.

1.1 Working of solar cell

A solar cell consists of two layers of semiconductor, one p-type and the other n-type, sandwiched together to form a 'p-n junction'. This p-n interface induces an electric field across the junction. When particles of light ('photons') are absorbed by the semiconductor, they transfer their energy to some of the semiconductor's electrons, which are then able to move about through the material. For each such negatively charged electron, a corresponding mobile positive charge, called a 'hole', is created. In an ordinary semiconductor, these electrons and holes recombine after a short time and their energy is wasted as heat.

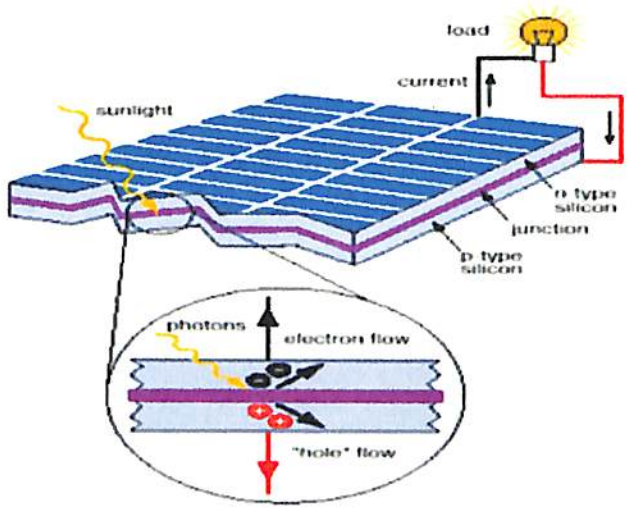


Fig.1 working of solar cell

In a solar cell, however, the electrons and holes near the p-n junction are swept across in opposite directions by the action of the electric field and others diffuse towards the junction to replace them. This separation of charge induces a voltage across the device. By connecting the device to an external circuit, the electrons are able to flow - and this flow of electrons is what we call electricity.[1]

1.2 Manufacturing technologies of solar cells

There are the following manufacturing technologies available.

1. **Crystalline silicon solar panel technology:** There are basically two different type of technologies (Based on the manufacturing technique used for silicon wafer)
   a. Mono crystalline silicon
   b. Multi crystalline silicon
2. **Thin film technology:** In thin film technology we used the following material
   a. Amorphous silicon(a-Si)
   b. Copper indium gallium diselenide (CIGS)
   c. Cadmium telluride (CdTe)
3. **Dye sensitized solar cell**
4. **Organic solar cell**

CHAPTER 2

Crystalline Silicon Technology

2.1 Introduction of crystalline technology

Crystalline silicon solar cells and modules have dominated photovoltaic (PV) technology from the beginning. They constitute more than 85% of the PV market today, and although their decline in favor of other technologies has been announced a number of times, they presumably will retain their leading role for a time, at least for the next decade.

Table 1 Silicon Thermal Properties[2]

Thermal Conductivity (solid)	1.412 W/cm-K
Thermal Conductivity (liquid)	4.3 W/cm-K
Specific Heat	0.70 J/g-K
Thermal Diffusivity	9 cm2/s
Melting Point	1683 K
Boiling Point	2628 K
Critical Temperature	5159 K
Density (solid)	2.33 g/cm^3
Density (liquid)	2.53 g/cm^3
Molar heat capacity	20.00 J/mol-K

Crystalline silicon solar cell technology has two types according to the use of the silicon crystal in manufacturing of silicon wafer.

- Mono crystalline silicon
- Multi crystalline silicon

2.2 Advantages of silicon wafer

Silicon is used because it is one of the most efficient semiconducting materials.

- Silicon is the most abundant element available on the earth crust. Almost 26% of earth's crust contains silicon in the form of silica and silicates.
- Unlike most other elements, silicon is a safe material to handle i.e. non toxic and non-hazardous for environmental safety and ecological aspects.
- Silicon is a highly chemically stable element which helps during its process treatment at high temperature.
- The silicon device technology is matured and well understood for last six decades compared to any other semiconductor including GaAs.

2.3 Limitations of silicon wafer

- Material cost is high.
- The energy pay-back period is high as it involves high energy process.
- The average efficiency in commercial production 10 to 16%.

2.4 Mono crystalline solar cell

Mono-crystalline silicon wafer is produced by slicing wafers of diameter 100 mm to 200 mm from high-purity single crystal ingots. The wafer having100 configuration normally cut into square shape and pseudo square having a shape 5"× 5" and 6"× 6". The p-type single crystal Si wafer having a 250±10 micrometer thickness.

There is no break in the structure, it is continuous. Growing large, continuous crystals like this is difficult and expensive. Solar cells that are made from a single unbroken crystal are called mono crystalline, meaning "ONE crystal"[3].

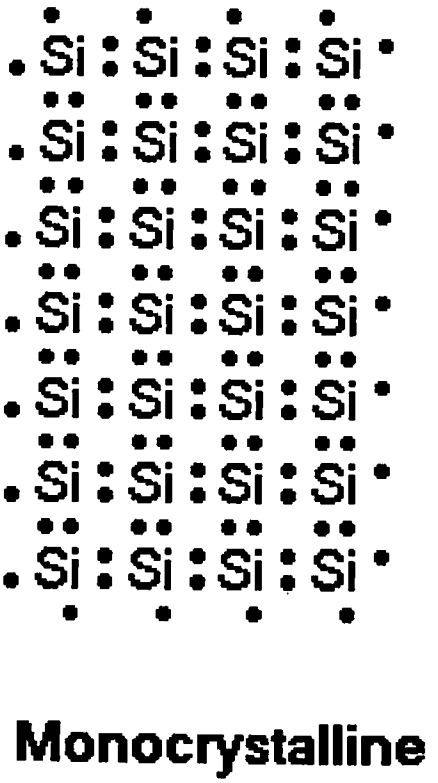


Fig 2: Mono crystalline silicon

2.5 Processes involved in manufacturing of mono crystalline solar cell[4]

Process 1	Polishing
Process 2	Texturisation
Process 3	Diffusion
Process 4	Plasma etching
Process 5	Phos Glass cleaning
Process 6	Post diffuse cleaning
Process 7	Oxide Passivation
Process 8	Front metal printing
Process 9	Back metal Contact
Process 10	Firing or Sintering
Process 11	Testing

Process 1: Polishing

Purpose

The purpose of polishing is to ensure that the wafers surface is free from any saw cut marks. It shall result in a polished & smooth surface.

Material Required

NaoH solution, DI water

Procedure

Load the Si- wafer in Teflon cassettes and when the temperature of 30% NaoH+DI water solution reaches between 90-100^{0}c. We put the cassettes in the solution and remove the cassettes from the solution in 30-40 seconds.

Precaution

1) Make the alkali solution very carefully.

2) Check the temperature of the solution before put the cassettes in the solution.

3) Remove the loaded cassettes from the solution very soon.

Process 2: Texturisation

Purpose

In this process we increase the surface area by texture structure of the Si wafer for maximum absorption of Sunlight. We know that by increasing the surface area, Isc(short circuit current) of the cell also increases.

Material Required

NaoH solution, Isopropyl Alcohol (IPA) solution and DI water etc

Procedure

First we loaded the wafer in to Teflon cassettes and at 79±1^{0}c temperature we put it into the tank which contains 0.5-0.6%NaoH+1.2% IPA + DI water solution for 25 minutes after then we put the wafer into the DI water. In this reaction IPA solution control the reaction and 0.5-0.6% NaoH solution slow the reaction.

Precaution

1) Make the solution very carefully.

2) Check out the temperature of the solution before put the wafer into the solution.

Process 3: Diffusion

Purpose

This process shall ensure proper uniform doping of the phosphorous paste on p-type silicon wafer to make it n-type. Therefore this method makes a p-n junction.

Material Required

Phosphorous paste, passivation furnace

Procedure

The texturised wafer is placed on printing chuck. The phosphorous paste is transferred on the silicon wafer with by using squeeze. The printed wafers are then placed on the conveyor belt of diffusion furnace by using tweezers. Conveyor belt has the speed 17.5 IPM. The furnace having three parts 1.Dryer Zone, which has three temperature region respectively 180^{0}c, 200^{0}c, 250^{0}c, 2.Firing Zone, which has three temperature region respectively 550^{0}c , 750^{0}c, 950^{0}c. 3.difusion zone, which has 5 temperature region and the temperature of last zone is 1020^{0}c.In diffusion zone flow N_2 and compressed air , flow of N_2 for +ve pressure, diffused

wafers are then collected on the receiver & undiffused wafer side is marked by quartz for identifications of p-type.

Precaution

1) Pate the phosphorous paste on the wafer very carefully.

2) Keep the diffusion paste bottle mouth clean and avoid any contamination

3) Use cotton /nylon gloves while loading the wafer in to the cassettes

Fig. 3: diffusion furnace process

Process 4: Plasma Etching

Purpose

After diffusion process the edge of the p-type layer and n-type layer shorted which is not required so to remove the shorted edge we do the plasma Etching process.

Material Required

Vacuum chamber, Freon gas, oxygen gas

Procedure

First we put the p-n junction in the pressurize machine and then put it into a vacuum furnace. Then at very high pressure flow Freon and oxygen gases. Freon gas has the property that it reacts in the presence of oxygen gas and then etches the edge of the entire p-n junction. So finally separate the p-n junction.

Precaution

1) pressure in vacuum chamber should be at desired level

2) presence of the oxygen is very necessary

Process 5: Phos Glass Cleaning

Purpose

After diffusion, a thick insulation layer of phosphorus glass is formed on the diffused surface, which needs to be cleaned.

Material Required

40% HF Solution, DI water

Procedure

The plasma etching wafers are loaded in a Teflon cassette. The cassettes are then dipped in 40% HF solution for 30-40 seconds and move up and down to remove phosphorus cycle. The cassettes are then transferred to DI water for rinse. They are once again rinsed in DI water. and finally they are fired in a dryer.

Precaution

1. Use cotton gloves before carrying out the operation.
2. Do not leave the diffused wafer in concentrated acidic solution for longer time is not more than prescribed time.
3. Diffused wafer must be loaded in absolutely dry carrier no water droplet should come in the wafer otherwise it will not remove prosperous.

Process 6: Post Diffusion Cleaning

Purpose

This process is done to ensure that the edge of isolated wafer surface is thoroughly cleaned to removing any type of contamination before sending the wafer for oxide passivity in order to improve and maintain the desired open circuit voltage of the solar cell.

Material Required

H_2O_2 solution, DI water, NH_3solution, acidic solution

Procedure

The Phos Glass cleaned wafers are loaded in Teflon cassettes. These cassettes are then dipped in the $NH_3+H_2O_2$ solution at 70^0c temp. for 10 minutes . These cassettes are then transferred to rinsing tank containing DI water. These cassettes are then dipped in acidic solution (0.5%HF solution) for one minute. They are again transferred to DI water for rinse. The wafers are then dried in the rinser dryer.

Precaution

1) Use surgical gloves before carrying out the operation.

2) Use measuring flask to measure chemicals for solution preparation.

3) Prepare fresh solution of base, and acid after fixed number of cycles.

Process 7: Oxide Passivation

Purpose

This process is to ensure the formation of SiO_2 layer on the diffused wafer. This layer passivity's the diagonal bonding of the Silicon, thereby reducing their recombination velocity. This improves the electrical properties of solar cells and also increases the life of cell.

Material Required

Quartz ladder boat and oxygen gas

Procedure

The wafers are placed back to back in a quartz ladder boat in such a way that the unmarked surface is exposed for passivation. This boat is then placed inside quartz tube using a glass rod having a 1400^0c temperature. Oxygen gas is allowed to pass though the tube so that it forms a $100A^0$ thickness of SiO_2 layer on the silicon wafers. This automatic furnace having a quartz ladder load which has a three zone .Then the passivated wafer is unloaded after 25minutes and kept at room temperature for cool down. By this the Isc and Voc of solar cell increase.

Precaution

1) Keep a proper check on the flow of oxygen flow meters.

2) Use gloves, masks & tweezers during operation.

3) Take proper care while loading the quartz ware.

Process 8: Front Metal Printing

Purpose

This process shall ensure an efficient front metal contact on n-side of the passivated silicon wafers.

Material Required

Polypropylene cassettes, Ag paste, Tweezers and front pattern

Procedure

The passivated wafers are loaded in polypropylene cassettes in such a way that the diffused side i.e., n-side of the wafers are printed with the given pattern. Two such cassettes are loaded in sender's platform keeping its n - diffused side upwards for printing. Some amount of front Ag paste is poured on the screen painter. Now the sensor senses the wafer and then automatically placed the wafer under printing chuck. These wafers are then passed through three infrared zones of temperature respectively 150.250,350^{0}c. The printed wafers are then obtained at receiver. Cell thickness of front metal paste ~80μm and 3mm distances between the horizontal lines.

Precaution

1) Use nylon/cotton gloves while loading the wafers.

2) Keep the rubber belt & print chuck clean.

3) Keep the paste covered to avoid any contamination.

4) Replace the pattern when it gives defective quality of print.

Process 9: Back Metal Print

Purpose

The wafers are printed back side with Ag just parallel to another paste in front side to get proper back ohmic contact & low series resistance of the cell.

Material Required

Al, Ag paste, Tweezers, Polypropylene cassettes and printing pattern etc

Procedure

The passivated wafers are loaded in polypropylene cassettes in such a way that its p-side is to be printed. Two such cassettes are loaded in sender's platform keeping its p - side upwards for printing. Sensors sense the wafers & they are automatically placed under the printing chuck. The paste is applied as thick strips by using squeeze. Theses wafers are then automatically passed on to belt having fixed speed. These wafers are then passed through the heating furnaces of different temperature range same as in previous step. The printed wafers are then obtained at the receiver.

Precaution

1) Use nylon/cotton gloves while loading the wafers.

2) Keep the rubber belt & print chuck clean.

3) Keep the paste covered to avoid any contamination.

4) Replace the pattern when it gives defective quality of print.

Process 10 : Back Metal Contact

PURPOSE

This process ensures a good back metal aluminum contact on the p-side of the wafer.

Material Required

Al paste, Polypropylene cassettes

Procedure

The wafers are loaded in polypropylene cassettes in such a way that its p-side is to be printed. Two such cassettes are loaded in a sender platform keeping its p-side upwards for printing. Sensor senses the wafer & they are automatically placed under the printing chuck. Al paste is poured over the nylon screen pattern. The remaining portion on the back side of the wafer is pasted wit Al by using squeeze. These wafers are then passed through the heating furnaces of different temperature ranges same as in front metal printing. The printed wafers are then obtained at the receiver.

Precaution

1) Use nylon/cotton gloves while loading the wafers.

2) Keep the rubber belt & print chuck clean.

3) Keep the paste covered to avoid any contamination.

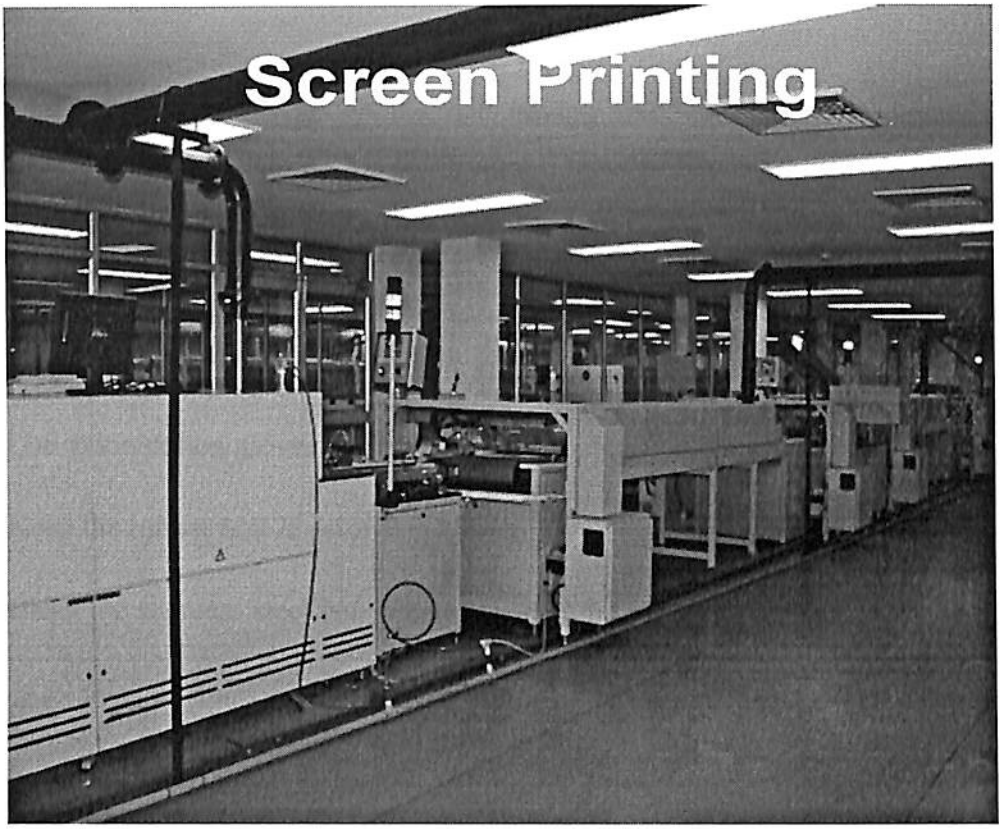


Fig. 4: screen printing of solar cell

Process 11: Firing or Sintering

Purpose

This process ensures a good ohmic contact between the paste and wafer otherwise no current will flow through it. It also lowers the solar cell resistance.

Material Required

Al baked wafer

Procedure

The printed wafers are placed on the belt having fixed belt speed by using Tweezers in such a manner that its n - side remains upside. These wafers are passed through different furnace of temperature ranges. The firing cells are obtained which are transferred for testing.

Precaution

1) Use nylon/cotton gloves while loading the wafers.

2) Keep the rubber belt & print chuck clean.

3) Clean the stainless steel belt once in a month by vacuum cleaner.

Process 12 : Testing

Purpose

This process ensures the current wise categorization of all solar cells at a fixed voltage. The solar cell below the acceptable current range shall be treated as rejected and sent for reprocessing.

Material Required

Fixed standard cell, processed cells Cotton gloves etc.

Procedure

The fired cells are placed one by one under the test chuck by allying bus bars of solar cells under the proves. The proves are then released to the cell. The light having its intensity equivalent to sunlight is allowed to fall from the test chuck. Test the cell's current at standard

480 mv with the help of potentiometer and panel meter .The chuck has to be maintained at a temperature of 25^0 Cwhile testing .at last place the wafers current wise in different boxes.

Precaution

1) Use gloves while handling the cell.

2) Never touch the reflected surface of light source with base hands.

3) Check the light intensity with the standard reference cell after every batch.

2.6 Preparation of Solar Module

In the preparation of solar module we have to collect the solar cells in a collected manner with their requirement. A single solar cell gives 0.5 volt. And we are taking the group of solar cells having same (Isc 4 Ampere). If we take 36 solar cells in series which gives 18 volt and give 72 watts. We take 18 volt because there will be some loss and not always in perfect condition so we take 18 volt so by reducing losses they produce near about 12 volt.

Step involved in the Preparation of the mono crystalline solar module [4]

Process 1	Front tabbing
Process 2	String
Process 3	Defluxing
Process 4	Visual Inspection
Process 5	Lay up
Process 6	Lamination
Process 7	Edge Formation
Process 8	Visual Inspection
Process 9	Channeling and Terminal Fixing
Process 10	Terminal Soldering
Process 11	Finishing

Process 1. Front Tabbing

Purpose

To solder the coated copper band over the bus bar printed on the solar cells we do front Tabbing.

Material Required

Soldering iron, power supply of 220volt, 50 Hz AC, solar cells, copper and liquid flux

Procedure

Take out the solder coated band of thickness and width and dip in a liquid for fixed time. Switch on the soldering iron. Take out the solar cells and solder the fluxed copper band on the brush bar of the cell with the help of soldering iron.

Precaution

1. The solar cell should not be broken.
2. There should not be dry soldering.

Process 2. String

Purpose

The purpose of this is to interconnect the front soldering solar cells of same current ranges.

Material Required

Tabbed solar cells

Procedure

Take out the string drawing affixed on glass plate corresponding to the cell to be laminated. Keeps the front side of solar cell facing downwards on the string. Tinned the solar cells downside up to 25 to 30 mm where tabs to be the soldered. Connect the side of the one cell with p-type of the other cell with n-type so that the electrical circuit is completed for series connections.

Precaution

1) The solar cell should not be broken.

2) There should not be dry soldering.

Process 3. Defluxing

Purpose

The purpose is to clean the solar cell string and make it free from the flux, contaminations, dust and any other foreign particle.

Material Required

Solar cells string, TCE vacuum connected string jig.

Procedure

Place the string on the float table and place the vacuum pick up on the solar cell strings.Place the string gently in the tray and remove the vacuum jig by switching off the solenoid valve. Dip the tray of the solution for 2-3 minutes. Rub the surface with hair brush. After that the tray is lifted up and hangs it over the hook until the solution stops falling. Transfer the jig to another zone for the drying under infrared light. Unload the string on the thermo Cole sheet for next stage operation.

Precaution

1. Refill the tank with fresh TCE after 30-40 strings.
2. The thermo Cole sheet should not contain any dust or contaminations.

Process 4. Visual Inspection

Purpose

To check the quality of string visually we do this process.

Material Required

Magnifying lens, lamp

Procedure

Place the string on the flat table to check that –ve polarity is on the left side and +ve on the right side check for the contaminations if found. Now send for defluxing. Check that the Cu bands are soldered in the bush bars of the solar cells.

Precautions

1. Do not mix the different current range of the solar cells.
2. Spared cell should be clean thoroughly cleaned TCE.

Process 5. Lay Up

Purpose

To arrange the solar cells string of various layers of the lamination and provide the termination.

Material Required

Solar cells, toughened glass, tedlar polyester sheet, EVA sheet and vacuum jig.

Procedure

Clean the glass with the TCE and place it on the table. Spread the EVA sheet on all sides of the glass plate. Place the string in the centre of EVA sheet that some space is left uniformly on all the sides. Place another EVA just above the solar cell string. Place the tedlar sheet over second EVA sheet and take out the end terminals through EVA and tedlar sheet at appropriate place .Tape the terminals with polyester and temperature resistant tape so that terminals are not distributed.

Precaution

1. Wear finger shells or gloves while layup.

2. Solar cells should not touch each other.
3. The string must remain in the centre.

Process 6. Lamination

Purpose

To protect the solar cells from environmental damage we do the lamination.

Material Required

Laminator

Procedure

Load the two lay-up modules in the laminator and close the top chamber. The module is laminated having time for 4 minutes, air bleed and pressing for rated time. These modules are sent to laminator at high temperatures. These modules are then allowed to cool. In the laminator EVA sheet melt spread over the glass to adhere the string b/w and tedler.

Precaution

1. The compressed air should not be less than 4-5 kg/sq-cm and there should be no dust particle in the laminator chamber.

Fig.5: lamination of the solar module

Process 7. Edge Formation

Purpose

To cut the excess lamination material from the spy module we do this step.

Material Required

Trimming knife, spy module, duster and IPA

Procedure

Remove the butter from the both sides of the module on trimming station and align with L-shaped fixed pattern. Cut the lamination paper from the side with the help of trimming knife. Rub edge and top L-bottom surfaces with duster to remove any contaminations.

Precautions

1. Handle the module carefully to avoid the any kind of damage.

Process 8. Visual Inspection

Purpose

To examine the visual defects in each laminated module.

Material Required

Work table, table lamp, magnifying glass.

Procedure

Place the string on the flat table to check that –ve and +ve polarity are on the left and right side respectively. Send for refluxing. Check that Cu bands soldered straight in the bush bars of the solar cells.

Precautions

- Handle module with care

Process 9. Channeling and Terminal Fixing

Purpose

To fix the mechanical frame to the laminated SPV module

Material Required

Work table, rubber anodize Al frame.

Procedure

Dispense the room temperature vulcanizing (RTV) Si rubber sealant in the both the L-shaped channel. Place the SPV module on the rubber sheet kept on the table and insert the L-shaped module to from a rectangle frame. Apply the RTV sealant on the groove of Al channel and also at the place from where the brush bars terminals are coming out in the order to properly seal the neck of the terminal.

Precautions

1) There should be no air gap b/w channel and glass.
2) The corners should be properly matched.

Process 10. Terminal Soldering

Purpose

To solder the bush bar terminal in the nylon terminal box

Material Required

TCE, solder wire, paste, flux

Procedure

Apply small amount of the flux brush on the –ve and +ve terminals of the terminals box. Does tinning of the terminals using solder wire. Solder the bush bar terminals of the terminals of the box using solder wire. Put the rubber washer in the box. Close the terminal box cover.

Precautions

1) The end terminals should not be left unsoldered.
2) The flux terminals should be cleaned properly withTCE.

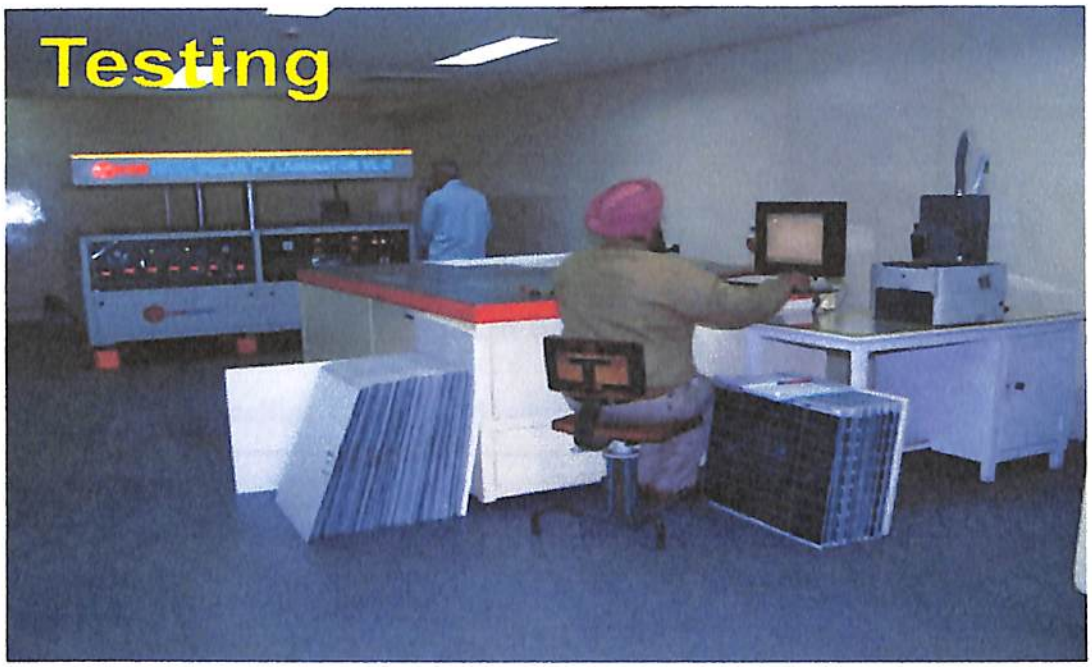


Fig.6: testing of the solar module

Process 11. Finishing

Purpose

To make the SPV module free from any strain marks, finger prints, contaminations and visual defects and fitting of the anodized Al channels.

Material Required

SPV module magnifying, cotton gloves, IPA tissue paper

Procedure

Place the SPV module on the work table and clean the SPV module thoroughly with tissue paper and IPA. Check the visual defects such as marks, strains, contaminations, improper, alignment and air bubble. If found mark then it sent for reprocessing

Precautions

- Do not mix the SPV module of different power rating.

Note: the solar panel manufacturing process of all kinds of the technologies is same after making the solar cell.

2.7 Mono crystalline solar cell and module specification

Table 2: mono crystalline 125mm*125 mm solar cell specification[4]

Material	Single Crystalline Silicon
Size	125 mm x 125 mm (Pseudo Square)
Surface	Textured
Thickness	240 + 30 Microns
Isc	4.5 Amp
Voc	600 mV
Im	4.0 Amp
Vm	480 mV
Pm	1.92 Watts
Fill Factor	70.0 %

Note :

1> There will be 8-10% increase in power after lamination using high transmission iron free glass and EVA (Ethylene Vinyl Acetate).

2> STC : Standard Test Condition

Solar Irradiation	AM 1.5
Intensity	100 milli Watt/cm 2
Cell Temperature	25 0 C
(Within the Measurement Tolerance of + 5%)	

Table 3: PM 80 mono crystalline solar module specification[4]

Electrical Parameters	PM 80
Maximum Power Rating Pmax. (Wp)	80.0
Minimum Power Rating Pmin (Wp)	75.0
Rated Current IMPP (A)	4.6
Rated Voltage VMPP (V)	4.6
Short Circuit Current Isc (A)	5.0
Open Circuit Voltage Voc (V)	21.5
No. of Cells (Nos)	36
Physical Dimension (mm) (L x W x T)	1200 x 550 x 35
Weight (Kg)	7.5
Maximum permitted module temperature (°C) -	40 to + 85
Maximum permissible system voltage v	600
Relative Humidity at 85°C (°C) x	600

Under Standard Test Conditions (STC): Air Mass AM 1.5, Irradiance 1000 W/m2, Cel Temperature 25°C

Nominal Operating Cell Temperature (NOCT) at : Wind Speed 1m/s, Irradiance 800 W/m2, Ambient Temperature 20°C

Table 4: 156mm*156 mm mono crystalline solar cell specifications[5]

Square length	156±0.5 mm
Diameter	200±0.5 mm(round chamfers)
Thickness	200+30 μm
Front surface	2mm Ag bus bar blue antireflecting nitride coating
Back surface	4mm Ag wide soldering pads Al surface field
Base terminal	P type mono crystal silicon wafer doped with boron
Junction	Phosphorous diffused N on P

Efficiency (η)	P_{mpp}(w)	V_{mpp}(V)	I_{mpp}(A)	V_{oc}(V)	I_{sc}(A)
17.4-17.5	4.17	0.514	8.175	0.622	8.910
17.3-17.4	4.14	0.510	8.116	0/618	8.846

156mm*156mm Cell engineering[5]

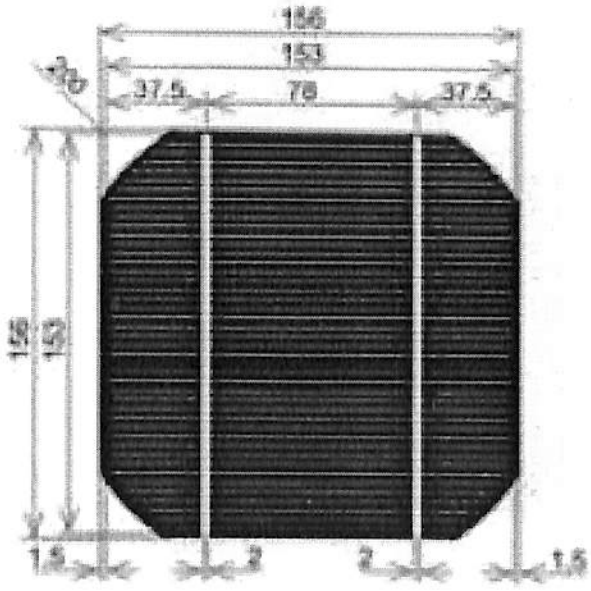


Fig. 7 mono crystalline solar cell (i) Front view

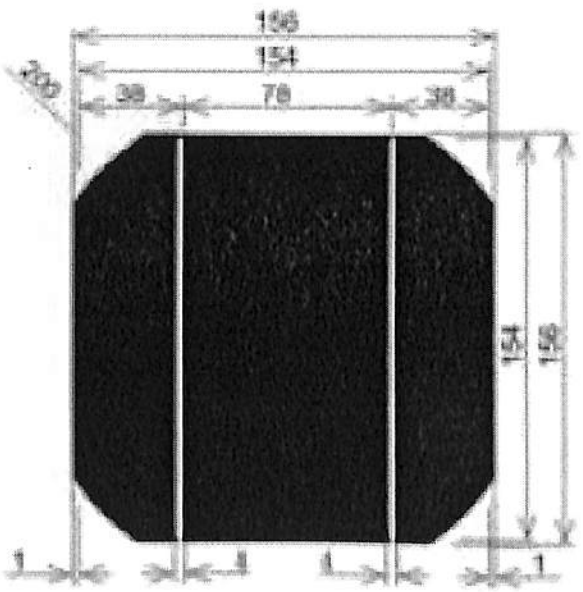


Fig.7(ii): Back view

2.8 Efficiency and cost of the mono crystalline solar panel

The conversion efficiency of solar cell is given by η= VmIm/solar power=FF*VocIsc/solar power, where Vm is the peak voltage, Im-peak current, Voc-open ckt voltage, Isc-short ckt current, FF- fill factor. FF should be unity but normally its range is 0.5-0.83

25% Efficiency of mono crystalline silicon cells already achieved by National Renewable Energy Laboratory (U.K.).the commercial efficiency of the solar cell lie in the range 12-16% less than one half of the fundamental. The module efficiency is slightly lower than that of the constituent cell due to area lost by frame and gap between cells. The module efficiency lies in the range of 10-16%. These are the most efficient and also the most expensive solar cells and the uniform color of the solar cell. The average cost of mono crystalline solar cell in India is Rs 140/watt[4].

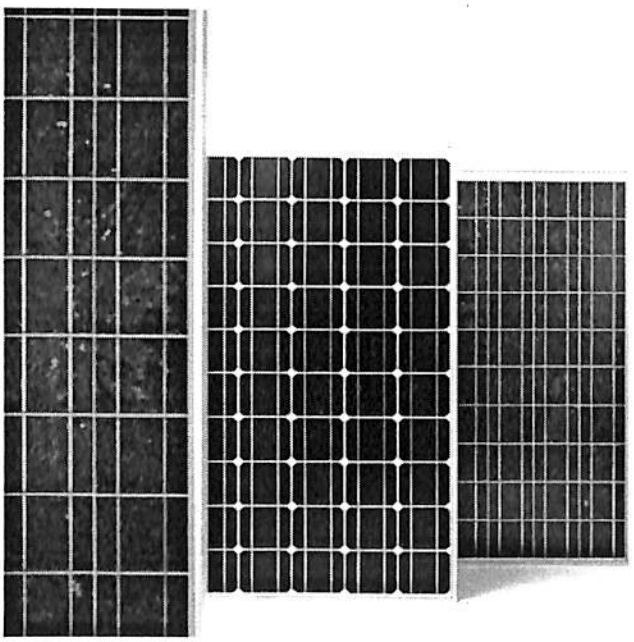


Fig 8: mono crystalline solar modules

CHAPTER 3

Multi crystalline silicon solar panel

3.1 Introduction

Multi crystalline silicon is obtained by a casting process in which molten silicon is poured into a mould and allowed to cool, then sliced into wafers. This process results in cells that are significantly cheaper to produce than mono-crystal cells, but whose efficiency is limited to less than 20% due to internal resistance at the boundaries of the silicon.

These are simply cells that are made of more than one crystal. The crystals are smaller than the ones used to make mono crystalline cells. Because they are smaller they are quicker and easier to grow. This then brings down the manufacturing cost for multi crystalline solar cells. We can see the different crystal regions in fig.9 because of their slightly different orientations they reflect light slightly differently, giving the patchy appearance of the cell. Each boundary between one crystal and the next has a tiny negative effect on the flow of electrons through the cell. The more boundaries there are, the poorer the electron flow[3].

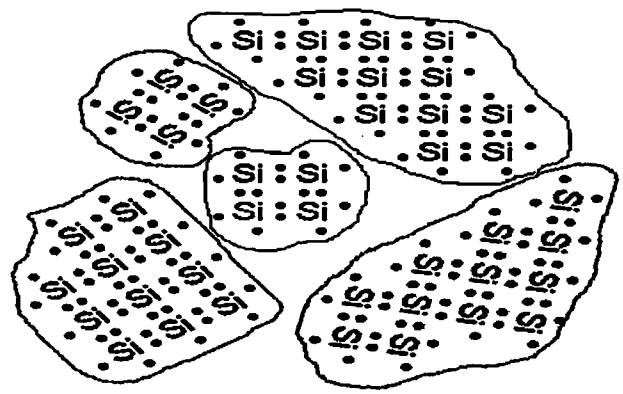


Fig.9 multi crystalline silicon

3.2 manufacturing of cell and module

The manufacturing process of solar cell and module of multicrystalline silicon is same as in moncrystalline silicon.

3.3 Cost and efficiency of the Panel

The commercial efficiency is around 10-12%. The efficiency in multi crystalline is decreased in comparison to mono crystalline. Each boundary between one crystal and the next has a tiny negative effect on the flow of electrons through the cell. The more boundaries there are, the poorer the electron flow the panel is cheaper than the mono crystalline silicon. In India the cost of the module is very less in comparison to mono crystalline.

3.4 Specification of multi crystalline solar module

Table 5: 156mm*156mm multi crystalline Silicon solar PV cell[6]

Electrical characteristics

Efficiency %	14.50
Maximum Power, Pmax (W)	3.52
Voltage at Pmax, Vmp (mV)	505
Current at Pmax, Imp (A)	7.00
Open Circuit Voltage, Voc (mV)	605
Short Circuit Current, Isc (A)	7.60

Mechanical characteristics:

Length and width	156±1 mm
Thickness	220+40(μm)
Front Contacts	Acid textured surface, anti-reflection coating, silver gridlines and two bus bars
Back Contacts	Fully covered aluminum BSF (Back Surface Field), two silver aluminum bus bars

156mm*156mm Cell engineering drawing[6]

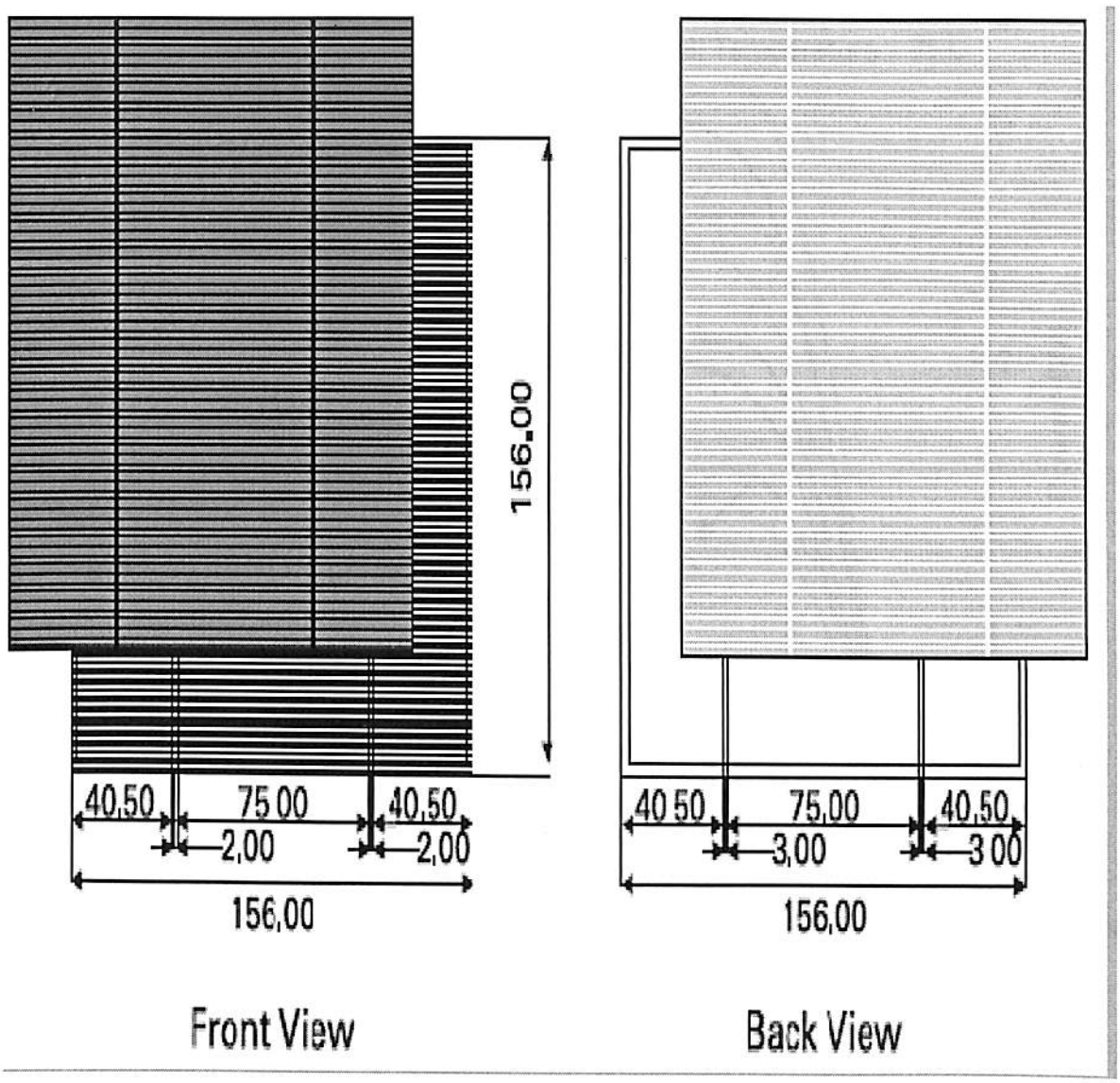
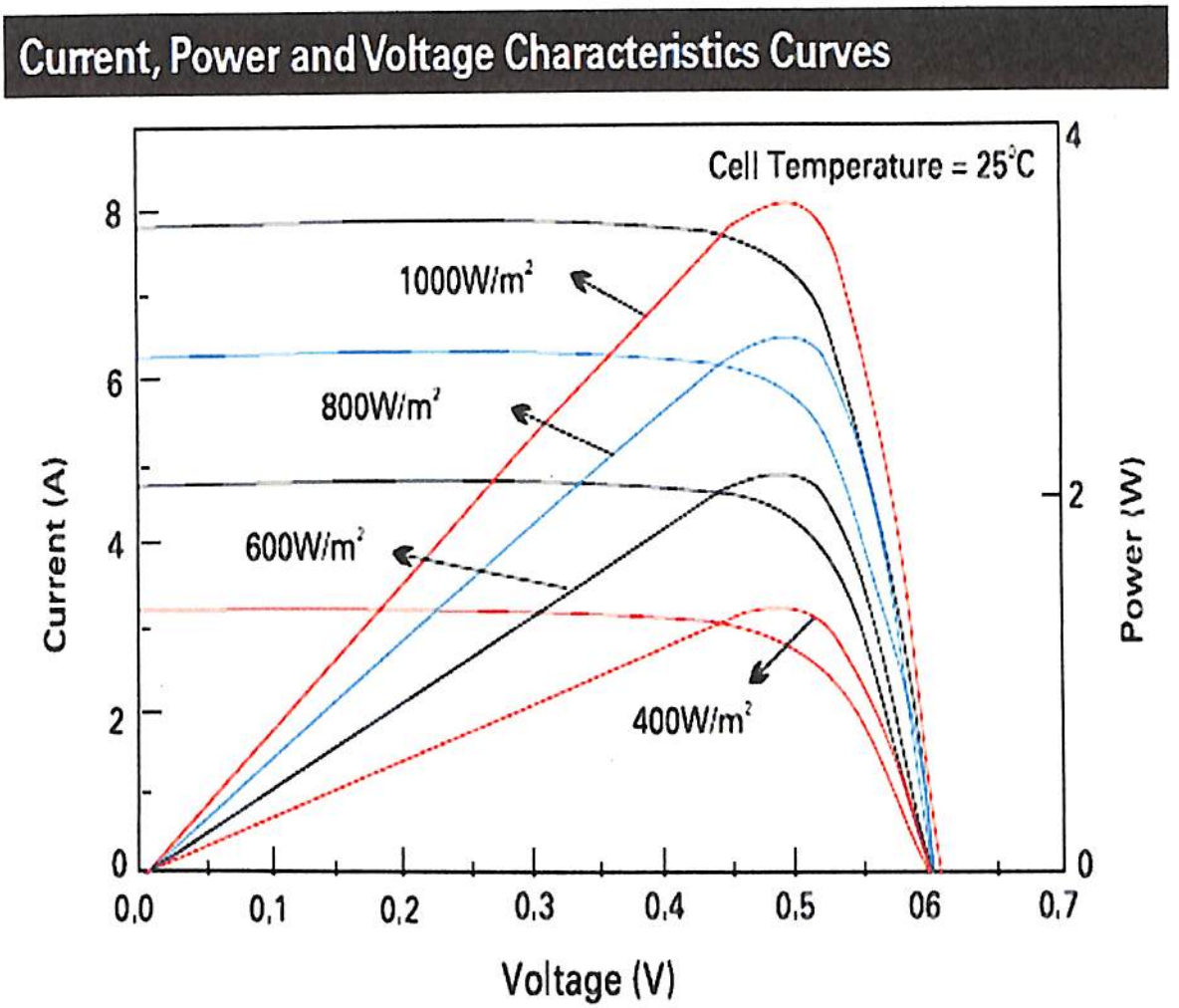


Fig.10: 156mm*156mm multi crystalline solar cell



Graph 1: current, power, voltage characteristics curve of 156mm*156mm multi crystalline solar cell[6]

Table.6: Multi crystalline solar module MBPV Max. Series 200 Wp and 230 Wp specification model No. MBPV-CAAP[6]

Electrical characteristic

Specification	200 Wp	230 Wp
Max.Power P_{max}(W)	200	230
Open ckt voltage V_{oc}(V)	36.25	36.83
Voltage at max. power V_{mp}(V)	28.78	30.91
Short ckt current I_{sc}(A)	7.7	7.95
Current at max. power I_{mp}(A)	6.95	7.95
Power tolerance %	±3	±3
NOCT^{0}c	47±2	47±2
Max. system voltage(IEC/UL) v DC	1000/600	1000/600
Max. series fuse rating(A)	15	

SCT-irradiation level 100w/m^2 spectrum AM 1.5, wind speed 1m/s, temp.-20^{0}c

Mechanical characteristics

No. of Solar cell and arrangement	Multi crystalline 156*156mm 6*10
Dimension	1661mm*971 mm*440 mm
Weight	43 kg
Front glass	High transmission, low iron, tempered & textured glass
Frame	Anodized Al frame with twin wall profile
Anodized thickness	17μ

Temperature coefficient

Temp. Coefficient of Max. power %/ K	-0.43
Temp. Coefficient of Open ckt voltage %/ K	-0.347
Temp. Coefficient of Short ckt current %/ K	0.11

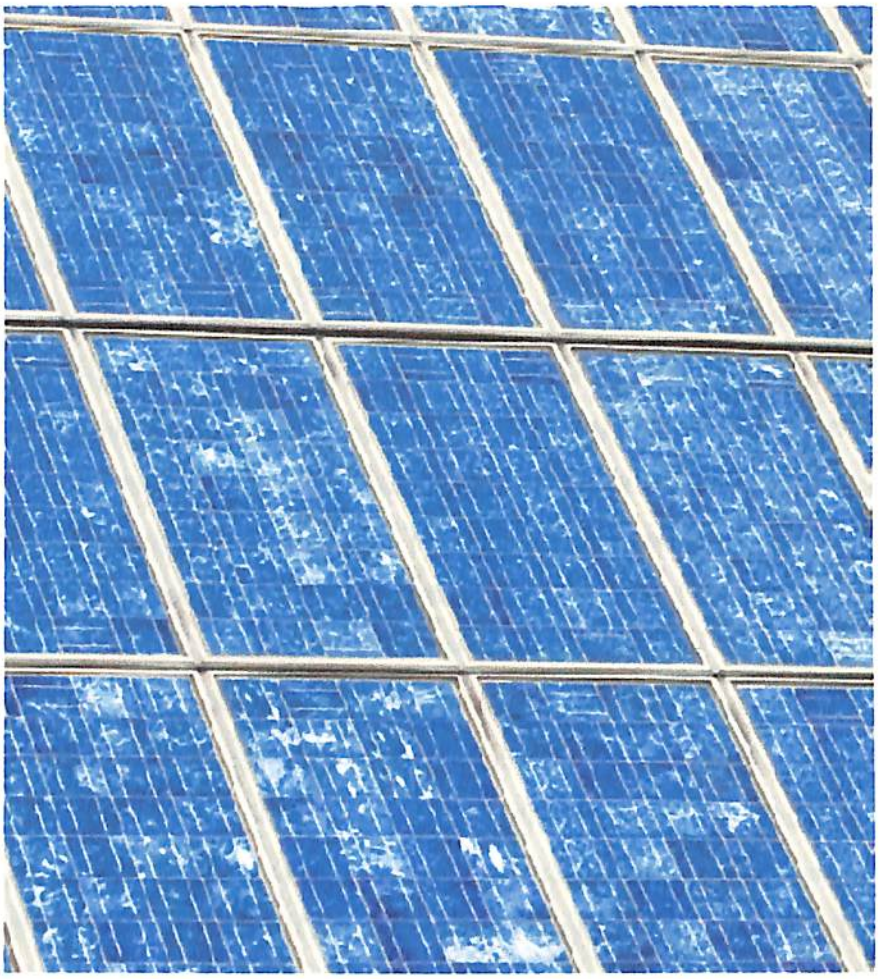


Fig. 11: multi crystalline solar panels

CHAPTER 4

Thin film technology

4.1 Introduction

The Thin film cells are constructed by depositing extremely thin layers of photosensitive materials on to a low cost backing such as glass, stainless steel or plastic. Thin-film silicon solar cells offset many of the disadvantages of conventional silicon cells by using a fraction of the pure silicon required in manufacturing solar cells. They are also easier to manufacture and easy to use in a variety of applications. The technology used in manufacturing thin-film solar cells is expected to be successful in achieving low manufacturing costs. However, the price advantage is counterbalanced by substantially lower efficiency.

Thin films use cheaply deposited semiconductor layers of the order of microns (1/1000 of a millimeter), and use less than 1% of the raw material (silicon) compared to wafer-based cells. Since the cells are deposited close to each other in the manufacturing process, the process does away with slicing individual wafers for cells, and assembling them together as modules. This implies fewer manufacturing steps required to create modules for final use.

There are following types of the material used in thin film technology

1. Amorphous silicon(a-Si)
2. CIGC(copper indium gallium diselenide)
3. CdTe(cadmium telluride)

4.2 Amorphous silicon (a-Si) thin film solar cells

Brief history

The first a-Si solar cell was developed by Carlson and Wronski in 1976. The ability to improve the stabilized efficiency of a-Si cells has become a major concern. Most improvements are based on the cell design, and stacked-cell shows a powerful tool to enhance the stabilized efficiency. In addition, the importance of light-trapping concepts and transparent conductive oxide (TCO) development are recognized in the a-Si cell design and fabrication.

Working of a-Si solar cell

Compared with the band gap of c-Si of 1.1 eV, a-Si offers a tunable band gap of 1.1~1.75 eV, which is controlled by the composition of the a-Si alloy. In addition, a-Si has a higher optical absorption coefficient than c-Si in the visible range of the spectrum so photoactive a-Si thickness can be much less than 1μm. Typical a-Si solar cells consist of a p- i- n (or n- i-p) diode structure, transparent TCO film (as front contact) and a metal film (as rear contact and back reflector)(Figure 12).

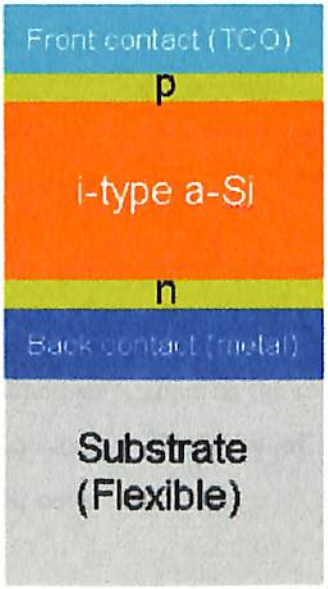


Fig12: structure of a-Si p-i-n junction solar cell

For the p- i-n structures, only the i-type layer is photovoltaically active with a typical thickness of between 200 and 500 nm. The p and n-type layers mainly serve to build an internal electrical field, and these layers are usually very thin (10~30 nm). The electrons and holes generated in the i-type layer are driven to the thin doping layers by the internal electrical field. This, the materials quality in the i-type layer mainly determine the a-Si solar cell performance. The defects in the i-type layer can cause charge carrier recombination loss and degrade the cell performance. In addition, because the electrical transport in i-type is assisted by the electrical field between p- and n type layer, the strength and distribution of the electrical field also influences the charge carrier collection and so determines the solar cell performance. The charged defect in the p/i and n/i interface regions can reduce the electrical field and change the electrical field distribution in the volume of i- layer and turns out to be crucial for solar cell optimization.

A simple way to reduce the effects of light- induced defects on carrier collection is to decrease the thickness of active intrinsic layer so that the light- generated carriers can reach the doped layers by traveling a shorter distance. However, the light absorption in i- layer will be lower with decreasing i- layer thickness. The stacked-cell can overcome the trade-off between the carrier generation and carrier collection and get more stable efficiency. The thin top cell in the stack has a strong built- in electrical field, while the thick bottom cell configuration is more stable because the top cell already reduces the light intensity of incident light. Besides the higher stability compared with the single-junction cell, stacked-cell can more efficiently utilize the solar spectrum by fabricating component cells using an a-Si alloy with different band-gaps.

The wide-band- gap top cells can mainly convert the blue and green parts of solar spectrum, while the bottom cell, with a narrow-band-gap, absorbs the red light that was not absorbed by the top cell. Therefore, the overall quantum efficiency of stacked cells can be improved compared with the single-junction a-Si cells[7].

4.2.1 Manufacturing process

The a-Si solar cells are deposited by plasma enhanced chemical vapor deposition (PECVD), which allows for the use of large area, flexible, and cheap substrates such as stainless steel, and polymer thin foils. At present, the industrial roll-to-roll deposition process of a-Si solar cells is limited by the low deposition rates and the cost of producing high-quality TCO layers. Thus, the price of a-Si solar modules is only marginally lower than that of crystalline silicon solar modules. However, as the data in Figure 13 shows, the production of a-Si modules is still increasing[7].

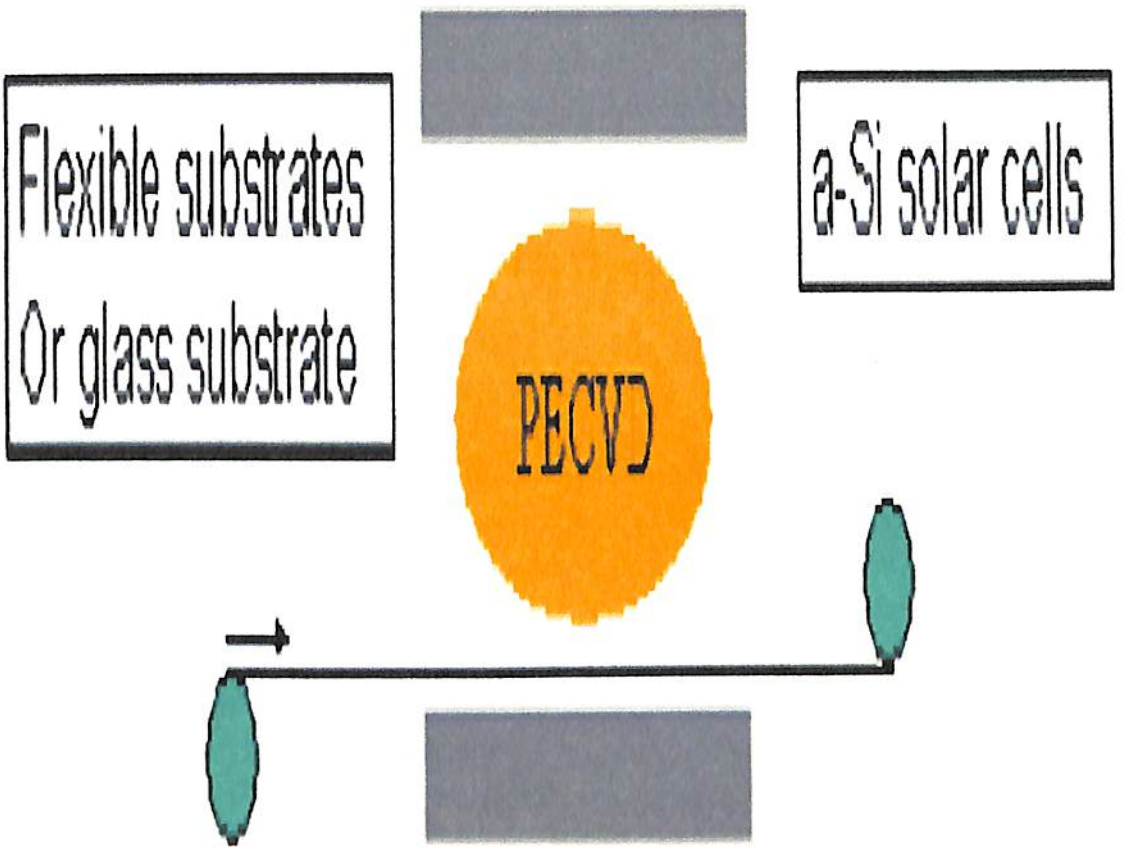


Fig 13: p-i-n in line a-si deposition

4.2.2 Advantage and disadvantage

New generation of Si solar cells using Si films less than 10 μm thick. Such a thin-film Si (TF-Si) solar cell offers many advantages that can lower the cost of generating solar electricity. A TF-Si cell offers (1) reduced bulk recombination leading to lower dark current, and higher *FF* of the device. Compared to a thick cell, a thin cell of the same material quality can yield higher device performance. Likewise, for a comparable performance, TF-Si solar cell requires lower material quality than a thick cell. It also offers (2) potential for low-cost cells/modules, (3) potential for lightweight photovoltaic's, (4) lower energy consumption for device fabrication, and (5) potential for flexible solar cells. (6) main disadvantage is lower efficiency of the solar cell[7].

4.2.3 Cost and efficiency of the a-Si solar module

Cost of the solar cell reduced in this technology due to less material used in the process but the overall efficiency of the cell is reduced. The efficiency of the solar cell in this technology is near 6%. The cost of the panel is around $2.13/watt.

4.2.4 Amorphous silicon thin film module specifications

Table 7: a-Si thin film solar module specifications[6]

Specification	Bin 345+15 W	Bin 330+15 W
V_{oc}(V)	191.17/187.5	192/187.8
V_{mp}(V)	1000	1000
I_{sc}(A)	3.02/2.9	2.9/2.8
I_{mp}(A)	2.7/2.4	2.9/2.8
Max.Power P_{max}(W)(initial/stablised)	413/345	395/330

NOCT-irradiation level 1000w/m^2 spectrum AM 1.5, wind speed 1m/s, temp.-20^{0}c

Module dimension

Weight	98 kg
Dimension l*w	2600*2200mm
Surface area	5.72 m^2
Frame design x-y	42*30mm

Temperature coefficient

Max. power %/ ^{0}c	-0.2
Open ckt voltage %/ ^{0}c	-0.33
Short ckt current %/^{0}c	-0.09
Max. Power voltage %/^{0}c	-0.32
Max. Power current% /^{0}c	0.14

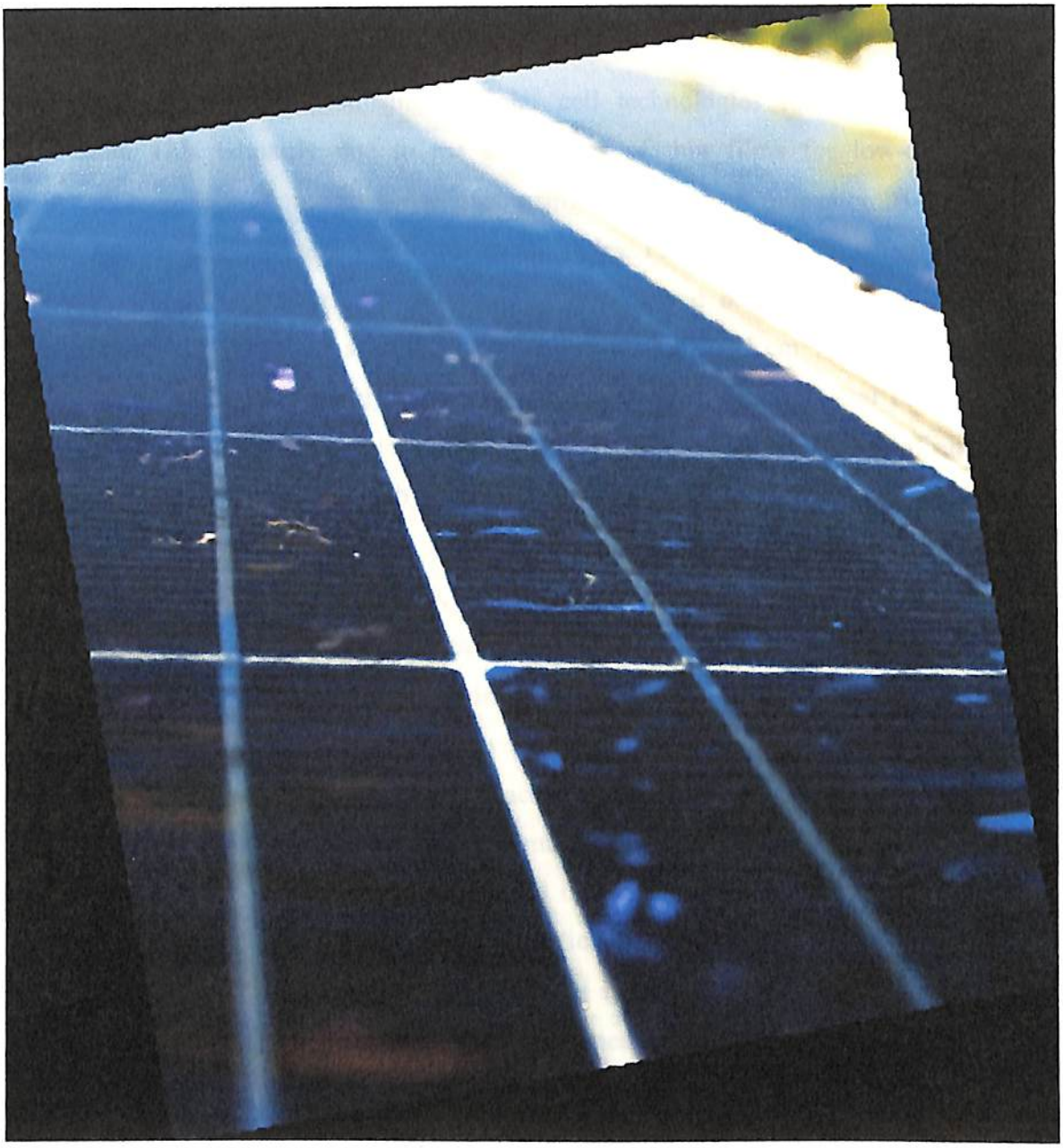


Fig.14: a-Si thin film solar panel

4.5 Copper indium gallium diselenide(CIGS) solar cell

Copper indium gallium diselenide Cu(InGa)Se2-based solar cells have often been touted as being among the most promising of solar cell technologies for cost-effective power generation. This is partly due to the advantages of thin films for low-cost, high-rate semiconductor deposition over large areas using layers only a few microns thick and for fabrication of monolithically interconnected modules. Perhaps more importantly, very high efficiencies have been demonstrated with Cu(InGa)Se2 at both the cell and the module levels. Currently, the highest solar cell efficiency is 45% with 0.5 cm^2 total area fabricated by the National Renewable Energy Laboratory (NREL) Furthermore, several companies have demonstrated large area modules with efficiencies >12% including a confirmed 13.4% efficiency on a 3459 cm^2 module by Showa Shell. Cu(InGa)Se2 solar cells and modules have shown excellent long-term stability in outdoor testing. In addition to its potential advantages for large-area terrestrial applications, Cu(InGa)Se2 solar cells have shown high radiation resistance, compared to crystalline silicon solar cells and can be made very lightweight with flexible substrates, so they are also promising for space applications.

The history of CuInSe2 solar cells starts with the work done at Bell Laboratories in the early 1970s, even though its synthesis and characterization were first reported by Hahn in 1953 and, along with other ternary chalcopyrite materials, it had been characterized by several groups. The Bell Labs group grows crystals of a wide selection of these materials and characterized their structural, electronic, and optical properties. The first CuInSe2 solar cells were made by evaporating n-type CdS onto p-type single crystals of CuInSe2. These devices were initially recognized for their potential as near-infrared photo detectors since their spectral response was broader and more uniform than Si photo detectors.

CIGS solar cell comes under the category of nano solar cell due the thickness of the layer of n and p type material.

The Boeing devices were fabricated using CuInSe2 deposited by coevaporation, that is, evaporation from separate elemental sources, onto ceramic substrates coated with a Mo back electrode. Devices were completed with evaporated CdS or (CdZn)S deposited in two layers with undoped CdS followed by an In-doped CdS layer that served as the main current-

carrying material. Throughout the 1980s, Boeing and ARCO Solar began to address the difficult manufacturing issues related to scale-up, yield, and throughput leading to much advancement in CuInSe2 solar cell technology. The two groups pursued different approaches to CuInSe2 deposition, which today remain the most common deposition methods and produce the highest device and module efficiencies. Boeing focused on depositing Cu(InGa)Se2 by co evaporation, while ARCO Solar focused on a two-stage process of Cu and In deposition at a low temperature followed by a reactive anneal in H2Se. The basic solar cell configuration implemented by Boeing provided the basis for a series of improvements that have lead to the high-efficiency device technology of today. The most important of these improvements to the technology include the following:

- The absorber-layer band gap was increased from 1.02 eV for CuInSe2 to 1.1–1.2 eV by the partial substitution of In with Ga, leading to a substantial increase in efficiency.
- The 1- to 2-μm-thick doped (CdZn)S layer was replaced with a thin, ≤50 nm, un doped CdS and a conductive ZnO current-carrying layer. This increased the cell current by increasing the short wavelength (blue) response.
- Soda lime glass replaced ceramic or borosilicate glass substrates. Initially, this change was made for the lower costs of the soda lime glass and its good thermal expansion match to CuInSe2. However, it soon became clear that an increase in device performance and processing tolerance resulted primarily from the beneficial in diffusion of sodium from the glass.
- Advanced absorber fabrication processes were developed that incorporate band gap gradients that improve the operating voltage and current collection. From its earliest development, CuInSe2 was considered promising for solar cells because of its favorable electronic and optical properties including its direct band gap with high absorption coefficient and inherent p-type conductivity.

As science and technology developed, it also became apparent that it is a very forgiving material since high efficiency devices can be made with a wide tolerance to variations in Cu(InGa)Se2 composition grain boundaries are inherently passive so even films with grain sizes less than 1 μm can be used, and device behavior is insensitive to defects at the junction

caused by a lattice mismatch or impurities between the Cu(InGa)Se2 CdS. The latter enables high-efficiency devices to be processed despite exposure of the Cu(InGa)Se2 to air prior to junction formation. High-efficiency CuInSe2-based solar cells have been fabricated by at least 10 groups around the world. While these groups employ a variety of processing technologies, all the solar cells have the same basic cell structure built around a Cu(InGa)Se2/CdS junction in a substrate configuration with a Mo back contact[2]

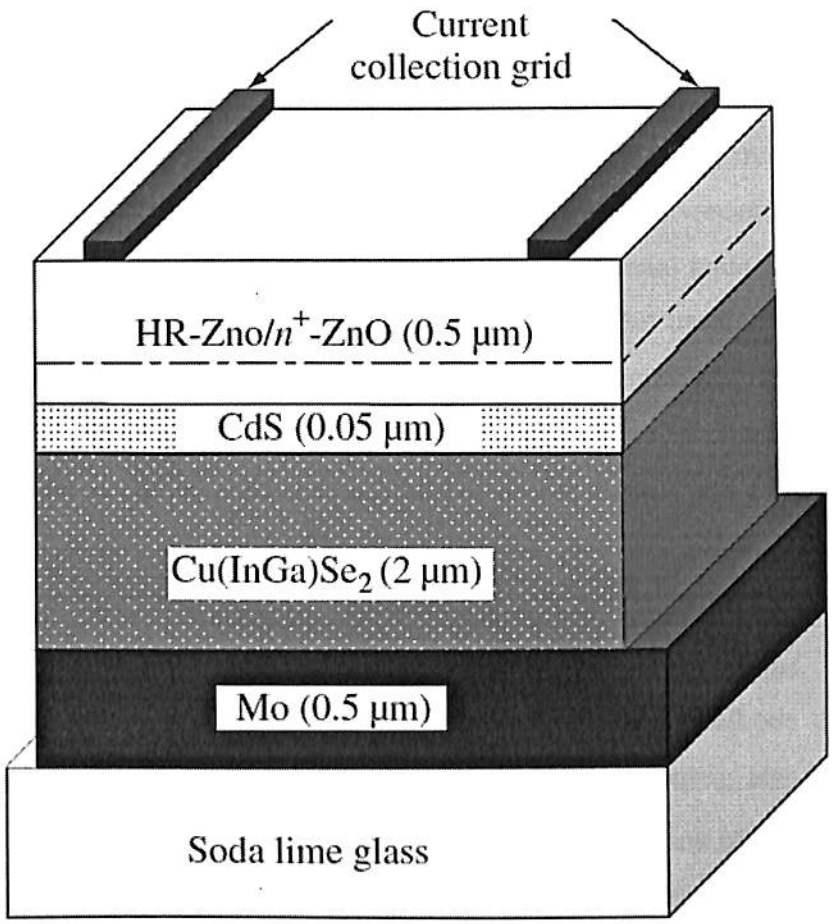


Fig. 15: shows a cross-sectional schematic of a standard device. This structure utilizes a soda lime glass substrate, coated with a sputtered Mo layer as a back contact. After Cu(InGa)Se2 deposition, the junction is formed by chemical bath–deposited CdS with thickness ≤50 nm. Then a high-resistance (HR) ZnO layer and a doped high-conductivity ZnO layer are deposited, usually by sputtering or chemical vapor deposition. Either a current-collecting grid or monolithic series interconnection completes the device or module, respectively

4.5.1 DEPOSITION METHODS

A wide variety of thin-film deposition methods has been used to deposit Cu(InGa)Se2 thin films. To determine the most promising technique for the commercial manufacture of modules, the overriding criteria are that the deposition can be completed at low cost while maintaining high deposition or processing rate with high yield and reproducibility. Compositional uniformity over large areas is critical for high yield. Device considerations dictate that the Cu(InGa)Se2 layer should be at least 1 μm thick and that the relative compositions of the constituents are kept within the bounds determined by the phase diagram, For solar cell or module fabrication, the Cu(InGa)Se2 is most commonly deposited on a molybdenum-coated glass substrate, though other substrate materials including metal or plastic foils have also been used and may have processing advantages.

The most promising deposition methods for the commercial manufacture of modules can be divided into two general approaches that have both been used to demonstrate high device efficiencies and in pilot scale manufacturing. The first approach is vacuum coevaporation in which all the constituents, Cu, In, Ga, and Se, can be simultaneously delivered to a substrate heated to 400 to 600°C and the Cu(InGa)Se2 film is formed in a single growth process. This is usually achieved by thermal evaporation from elemental sources at temperatures greater than 1000°C for Cu, In, and Ga. The second approach is a two-step process that separates the delivery of the metals from the reaction to form device-quality films. Typically the Cu, Ga, and In are deposited using low-cost and low temperature methods that facilitate uniform composition. Then the films are annealed in a Se atmosphere, also at 400 to 600°C. The reaction and anneal step often takes longer time than formation of films by coevaporation due to diffusion kinetics, but is amenable to batch processing. High process rate can be achieved by moving continuously through sequential process steps or with a batch process whereby longer deposition or reaction steps can be implemented by handling many substrates in parallel.

4.5.2 Substrates

Soda lime glass, which is used in conventional windows, is the most common substrate material used for Cu(InGa)Se2 since it is available in large quantities at low cost and has been used to make the highest efficiency devices. Cu(InGa)Se2 deposition requires a substrate temperature (TSS) of at least 350°C and the highest efficiency cells have been fabricated using films deposited at the maximum temperature, TSS ≈ 550°C, which the glass substrate can withstand without softening too much. The glass is electrically insulating and smooth, which enables monolithic integration into modules. The soda lime glass has a thermal expansion coefficient of 9×10–6/K, which provides a good match to the Cu(InGa)Se2 films. The glass composition typically includes various oxides such as Na_2O, K_2O, and CaO. These provide sources of alkali impurities that diffuse into the Mo and Cu(InGa)Se2 films during processing, However, a process that provides a more controllable supply of Na than diffusion from the glass substrate is preferred. This can be achieved by blocking sodium from the substrate with a diffusion barrier such as SiOx or Al2O3. Then sodium can be directly provided to the Cu(InGa)Se2 growth process by depositing a sodium-containing precursor layer onto the Mo film. Commercially available soda lime glass may also contain significant structural defects that can adversely impact module production. Borosilicate glass does not contain the alkali impurities and may have fewer structural imperfections but has a lower thermal expansion coefficient, 4.6 × 106/K, and is more expensive.

4.5.3 Back Contact

The Mo back contact, used for all high-efficiency devices, is typically deposited by direct current (dc) sputtering. The thickness is determined by the resistance requirements that depend on the specific cell or module configuration. A film with thickness 1 μm will typically have a sheet resistance of 0.1 to 0.2 a factor of 2 to 4 higher resistivity than bulk Mo. Sputter deposition of the Mo layer requires careful control of the pressure
to control stress in the film and to prevent problems such as poor adhesion that it might cause. During Cu(InGa)Se2 deposition, a MoSe2 layer forms at the interface.

Its properties are influenced by the Mo film with less MoSe2 forming on dense Mo, sputter-deposited under low pressures. This interfacial layer does not necessarily degrade device performance. Metals other than Mo have been investigated with limited success.

4.5.4 JUNCTION AND DEVICE FORMATION

The first experimental device that indicated the potential for CuInSe2 in high-performance solar cells was a heterojunction between a p-type single crystal of CuInSe2 and a thin film of n-type CdS . Consequently, in the early thin-film work the junction was formed by depositing CdS on the CuInSe2 films. The device was further developed to contain an undoped layer of CdS, followed by CdS doped with In, both deposited by vacuum evaporation A conformal and pinhole-free coating of this thin CdS layer is obtained by using chemical bath deposition to make the CdS buffer layer.

Chemical Bath Deposition

Chemical bath deposition (CBD) of thin-film materials can be viewed as a chemical vapor deposition (CVD) in the liquid phase instead of the gas phase. It is also referred to as solution growth. The method has been used in particular for chalcogenide materials such as PbS , CdS, and CdSe . A variety of precursor compounds or ions can be used to deposit a specific compound. Deposition of CdS buffer layers on Cu(InGa)Se2 is generally made in an alkaline aqueous solution (pH > 9) of the following three constituents

1. cadmium salt; for example, CdSO4, CdCl2, CdI2, Cd(CH3COO)2
2. complexing agent; commonly NH3 (ammonia)
3. sulfur precursor; commonly SC(NH2)2 (thiourea).

The concentrations of the various components of the solution can be varied over a range and each laboratory tends to use its own specific recipe

The Cu(InGa)Se2 film is immersed in a bath containing the solution and the deposition takes place in a few minutes at a temperature of 60 to 80∘C. This can be done either by immersion in a room-temperature bath that subsequently is heated to the desired temperature or by preheating the solution. The reaction proceeds according to the formula

$Cd(NH_3)_4^{2+} + SC(NH_2)_2 + 2\,OH^- \rightarrow CdS + H_2NCN + 4\,NH_3 + 2\,H_2O$

4.5.5 Advantage & disadvantage of nano solar cell[8]

Advantages

- Nano solar cells (CIGS cell) require 1/50th to 1/100th of the total raw materials needed for a typical silicon solar cell.
- Nano solar cells remove the obstacle the solar industry currently faces in the shortage of silicon for wafers.
- CIGS is superior to amorphous Silicon (a-Si) and Cadmium Telluride (CdTe) by achieving higher conversion efficiencies.
- CIGS modules have demonstrated reliable and stable field performance for nearly 20 years.
- Cost. Flexible solar is leading the way to cheap energy from the sun. Costs for this technology are dropping quickly and with the investment in research and development, these costs will continue to fall.
- Application. The biggest advantage currently with thin film solar is its numerous application options. Unlike traditional panels, flexible panels can be applied to a wide variety of surfaces. In addition to the traditional roof mounted design, these cells are being molded to cars, backpacks, clothing, and even windows. Some companies are even integrating the cells into things like roof tiles and siding, so your house will have solar in it, not just on it.
- Technology Advancements. Many large companies such as Shell, Honda, and Nanosolar are throwing all their research muscle behind thin film solar. This means that the technology will improve greatly over time, and some of the advancements are already coming to market.

- Fewer Defects. Because the manufacturing process is simpler, there are often fewer defects. The highly technical method of building traditional solar panels, sometimes compared to computer chip manufacturing, involves a lot of detailed soldering. This has been historically a place where the traditional panels experienced a lot of warranty issues. Not so with solar film. The process is closer to printing and therefore is subject to fewer defect issues.
- Less Voltage Drop. Electricity in most applications flows better when its cool. When thin film solar cells heat up they tend to lose less voltage than traditional panels.
- Performance in Low-light. Many thin solar panels have better energy production in low-light and shading situations.
- Durability. Since the technology is fairly new, there are some questions about how long these cells will last. But many early-adopters have reported their cells lasting 15 years and more. These cells do not require the glass and aluminum casings of traditional cells because the materials within them are flexible and malleable, not brittle like crystalline silicon. This means they will likely take more abuse and last longer

Disadvantages:

- Efficiency: Efficiency of these cells has lagged anywhere from 50%-70% behind that of traditional crystalline cells. This is changing quickly however. In 2005, the National Renewable Energy Lab achieved a world record 45% efficiency for a CIGS cell. This means that 45% of the total energy that fell on the cell was converted to electricity. This is approaching the world record for a common solar panel of 24.7%.
- Heat Retention. Because thin film solar is usually applied directly to a surface, they can retain more heat. Traditional panels are generally installed with a standoff, meaning there is space between the panel and the supporting surface, allowing for air to cool the panels. Thin film solar may retain more heat, creating a balance act between this and its benefit of better performance at higher temperatures.

4.5.6 CIGS Solar module specification

Table 8: 128/144/158 CIGS solar module specification[9]

Cell crystalline CIGS on to stainless steel foil

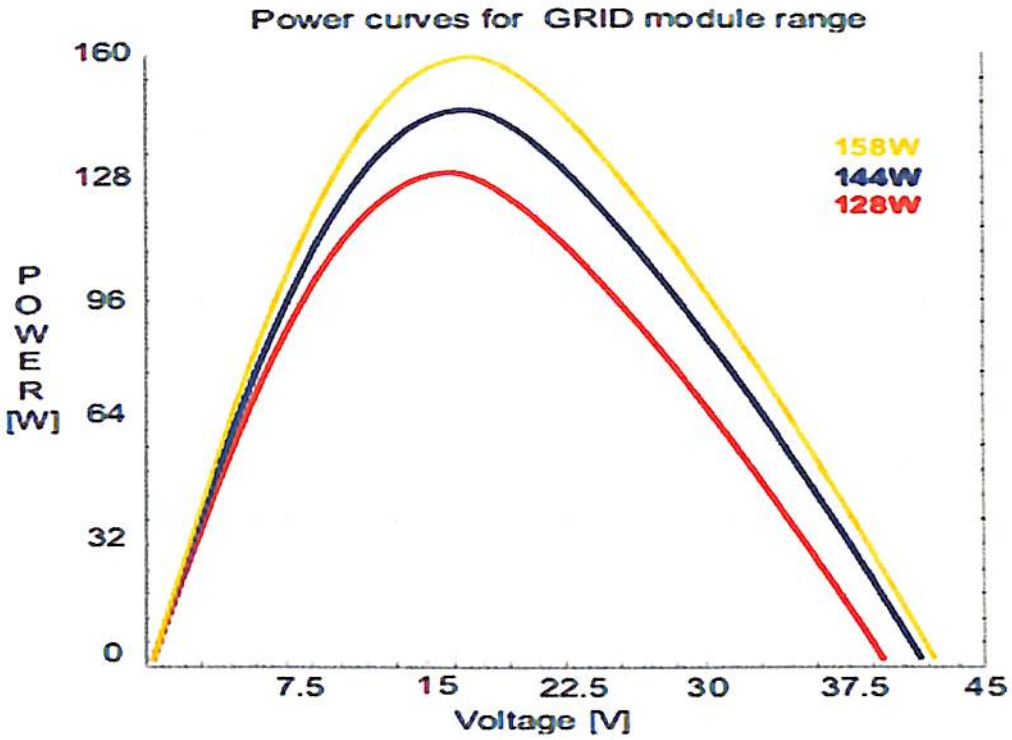
Specification	SE 128MP-BG1418B	SE 144MP-BG1418B	SE 155MP-BG1418B
V_{oc}(V)	39.6	41.6	42.4
V_{mp}(V)	25.6	27.2	28.8
I_{sc}(A)	6.4	6.6	6.8
I_{mp}(A)	5	5.3	5.5
Power at STC P_{max}(W)	128	144	158

NOCT-irradiation level 800w/m^2 spectrum AM 1.5, wind speed 1m/s, temp.-20^0c

Module dimension

Weight	21.8 kg
Dimension a*b	874mm*1909 mm
Mounting oblong hole of the module g*f	8mm*9.5 mm
Module design(c) (distance b/w mounting hole)	800mm
Module design(d) (distance from the corner)	554.5 mm
Frame design x-y	42mm*30mm

Power and voltage curve for CIGS solar module[9]



Graph 2: power and voltage curve of CIGS solar module

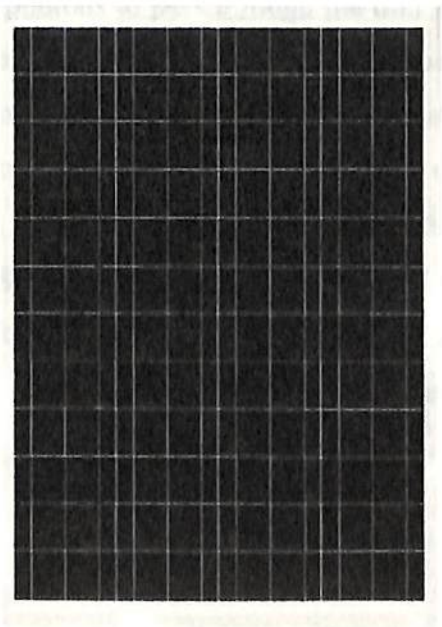


Fig.16: CIGS solar module

4.6 Cadmium Telluride solar cell (CdTe)

Introduction

The present invention relates to methods of making polycrystalline CdTe/CdS thin film solar cells and especially such methods which make inexpensive mass production possible. Because of its favorable energy gap of 1.45 eV, CdTe is ideally suited as photo-active material for solar cells. Moreover, polycrystalline layers of a few μm thickness can be made by various methods (physical or chemical evaporation/sublimation in a vacuum, electrolytic deposition, screen printing, spray methods), which in general are subjected to a chemical-thermal post-treatment to improve their electronic properties. These two characteristics make CdTe one of the most interesting candidates for inexpensive thin film solar cells.

Manufacturing process

A typical CdTe solar cell construction is shown in Figure 17. In these cells, a layer (~2 μm) of p-type CdTe (p-type character arising due to a slight non stoichiometry of Cd in the semiconductor) is joined to a thin layer (~0.1 μm) of n-type CdS to form the hetero junction. The CdS layer, having a energy gap in excess of 2.4 eV, acts as a window allowing a majority of the incoming photons to pass through the thin layer. The incoming photons then impinge on the CdTe layer which, having an adsorption coefficient of greater than 105 cm-1 (Figure 17 and band gap of 1.45 eV, is well suited for the absorption of photons from within the solar spectrum. In fact it has been shown that a layer of only a few mm in thickness is sufficient to absorb more than ninety percent of light with energy above the band gap. To complete the cell the CdS layer is joined to a layer of TCO (typically consisting of SnO2) which is then connected to an electrical contact. Electrical connection at the back of the cell can be made by a metallic contact, as there is no requirement of transparency.

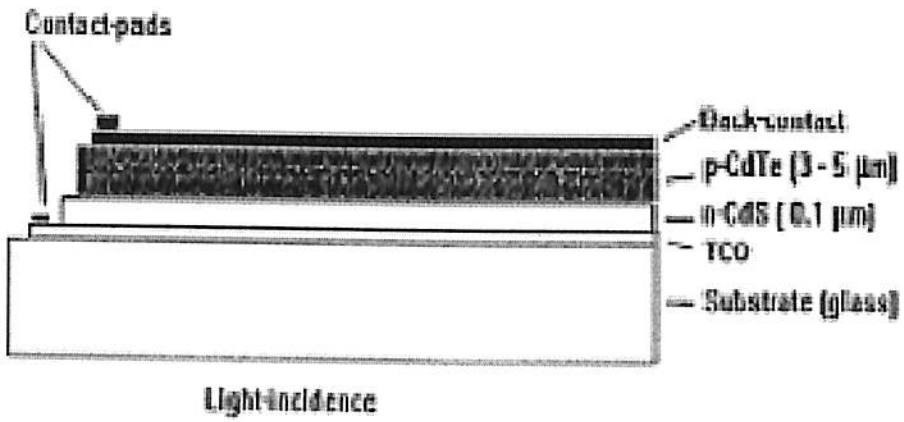


Fig.17: CdTe solar cell

CdTe cells with a laboratory efficiency as high as 16.5 percent have been developed at NREL using a modified CTO/ZTO/CdS/CdTe cell structure. In these cells the typical TCO layer of SnO2 is replaced by Cd2SnO4 (CTO), which has both a lower resistivity and higher transparency. Furthermore, the addition of a buffer layer of zinc stagnate (Zn2SnO4, or ZTO) was shown to improve cell performance by an inter diffusion process in which Zn from the ZTO layer alloys with the CdS, increasing the band gap of the window layer and improving the blue quantum efficiency. These modified cells have a fill factor in excess of 73% with a V_{OC} of 0.84 V and I_{SC} of 26.1 mA/cm2.

One of the major benefits of CdTe thin film photovoltaic cells is the multitude of manufacturing techniques that can be used to produce the films, many of which are very promising for large-scale production. These techniques include sputtering, chemical vapor deposition (CVD), atomic layer epitaxy, screen-printing, galvanic deposition, chemical spraying, close-packed sublimation, modified close-packed sublimation, and sublimation-condensation. Each of these processes allow for unique control of film qualities and are all scaleable to varying degrees. For example, processes such as CVD allow for enhanced control over the concentration and distribution of dopants such as P and As but at the same time have a high cost, toxicity, and are inefficient in materials use especially of the dopant gases[7].

CHAPTER 5

Dye Sensitized Solar Cells (DSSC)

5.1 Introduction

Dye-sensitization, the basis for dye solar cells, has its historical origin in the 19th century, when photography was invented by Vogel in Berlin 1873. However, the use of dye - sensitization in photovoltaic remained rather unsuccessful until the early 1990's. Grätzel and co-workers have developed the so called dye sensitized nano structured solar cell, or the Grätzel cell, with an energy conversion efficiency exceeding 7% in 1991 by combination of nano structured electrodes and efficient charge injection dyes[7].

The dominance of inorganic solid-state junction, usually made of Silicon, is now being challenged by the emergence of a third generation of solar cells, based e.g. on nano crystalline and conducting polymer films.

5.2 Working Principle[7]

Nano crystalline DSSC, based on the mechanism of a fast regenerative photo electrochemical process, convert sunlight into electricity as a conventional cell made of Si does. Unlike Si cells, the functional element, which is responsible for light absorption (the dye), is separated from the charge carrier itself. In the case of a n-type semiconductor, TiO 2 (bandgap 3.2 eV), the dye gets excited by adsorbing an photon, injects the electron into the TiO2, which then can be extracted at the front electrode (a transparent TCO glass) as an external current. The dye on the other hand is subsequently reduced by a redox electrolyte, which consists of an organic solvent and the redox couple iodide/triiodide.

The electrolyte also drives the charge transport between the counter electrode (also TCO glass) and the dye molecules. The counter electrode is covered with some Pt, which acts as a catalyst for the redox reaction, to get a low-resistant electron transfer. It can be shown that only the dye molecules directly attached to the surface of the semiconductor are able to inject charge carriers efficiently into the semiconductor.

5.3 Manufacturing process[7]

The standard way of preparing the DSSC in the laboratory is sandwiching the different cell layers between two glass plates, the substrate and the superstrate, which is usually the TiO2 electrode (Fig.No.18). In order to minimize manufacturing costs in mass production, the single cells should be prepared between one common glass plate with large surface area, as it is already done in commercial thin film modules. Furthermore Kay and Grätzel (1996) developed a three layer monolithic cell structure (Figure 18) to adapt more processing benefits of the thin film solar cell technology, so that the commercialization can be realized. In the monolithic structure, all the layers of the cell can be deposited on top of each other on a single TCO coated glass plate, while the opposite glass plate without TCO coating serves merely as a protective barrier and encapsulation.

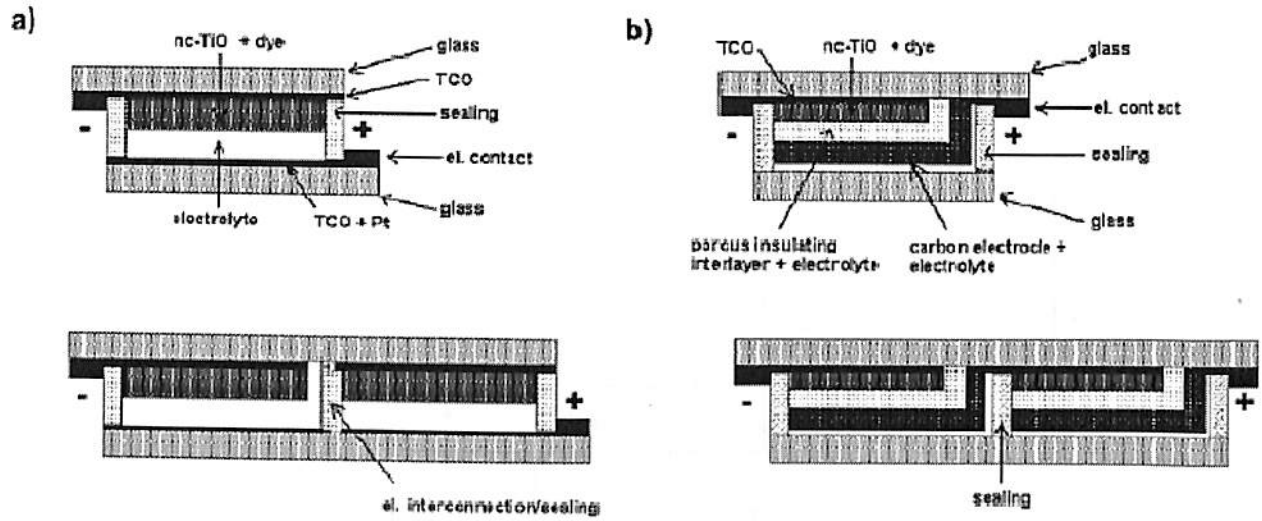
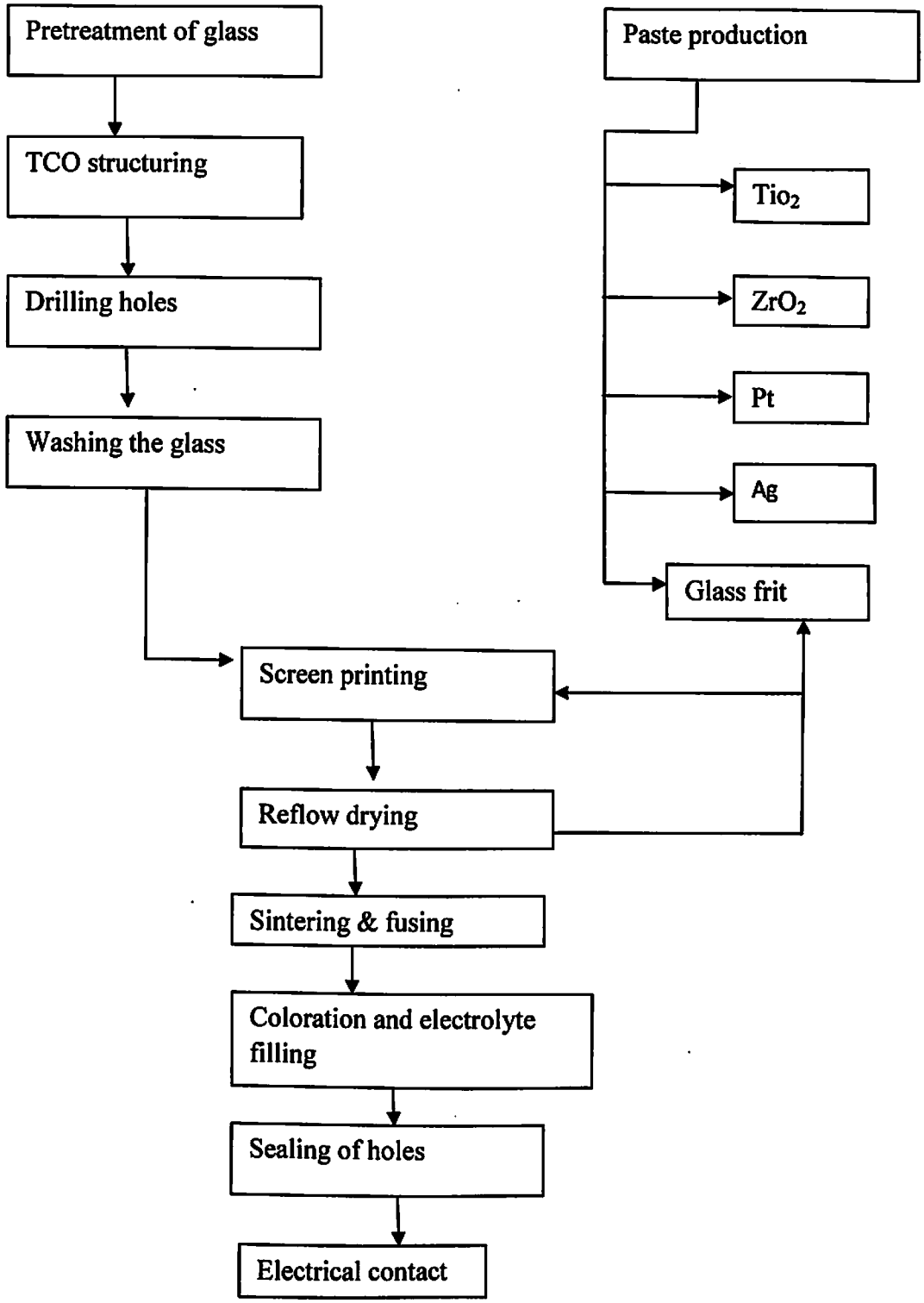


Fig.18: the two main DSSC cell (upper) and module (lower) architectures: a) the sandwich structure b) the monolithic structure.

Considering mass production, the use of flexible transparent plastic substrates could offer an advantage over glass substrates. Flexible substrates could be used in continuous roll to-roll process, making it possible to produce photovoltaic cells in large quantities and at high throughput, and thereby substantially lower costs.

The following fig.19 shows the manufacturing process of DSSC [7]



5.4 Advantages/Disadvantages DSSC[7]

One of the major advantages of the DSSC technology over other PV technologies is the relatively simple manufacturing processes and the inexpensive equipment and facilities needed. Old-fashioned screen-printing machines can be used compared to the expensive clean room facilities needed for semiconductor processing. Furthermore materials of the cells may become cheap in a large -scale production (at present, costs are significant for cell elements like the dye and the Pt catalyst at the back contact).

Since the dye solar cells are printed on foil, they are flexible and therefore can be adapted to almost any shape. They don't have to reach such high efficiencies achieved from Si solar cells, as they can be used in other ways. For example they can be effectively used by adding them into the window glass of a building, and therefore distributed over a larger area rather than just put up on the roof.

To become an economically viable and commercially feasible technology, the dye sensitized solar cells should be capable of maintaining non-degrading performance in operating conditions over several years, preferentially tens of years. However, the question of long-term stability of the dye -sensitized solar cells seems to remain unsolved thus far. Potential sources of degradation in the cell are for example, changes in the surface structure of the TiO 2, or photo-chemical or chemical degradation of the dye.

5.5 Efficiency of DSSC[7]

The high energy conversion efficiencies performed by the dye -sensitized solar cells is one of the reasons for the rapidly expanded interest in DSSCs. Several published results are listed in Table 9

Semi-conductor	Dye	η (%)	area (cm^2)	illumination (mW/cm^2)	reference
TiO_2	?	11	0.25	100 (AM1.5)	Green 2001
TiO_2	Black Dye	10.4	?	100 (AM1.5)	Grätzel 2000
TiO_2	N3	10.0	0.3	96 (AM1.5)	Nazeeruddin et al. 1993
TiO_2	N719[22]	9.2	1.5	? (AM1.5)	Deb et al. 1998
TiO_2	$RuL_2(\mu\text{-}(CN)Ru(CN)L''_2)_2$	7.1 7.9	0.5	75 (AM1.5) 8 (AM 1.5)	O'Regan & Grätzel 1991
TiO_2	N3	6 7.3	1	100 (ELH lamp) 11.5 (ELH lamp)	Hagfeldt et al. 1994
TiO_2	A Ru -phenantroline derivative	6.1	0.44	100 (AM 1.5)	Yanagida et al. 2000
TiO_2	a coumarin derivative	5.6	?	100 (AM1.5)	Hara et al. 2001a
TiO_2	Cu-2-α-oxymesoisochlorin	2.6	0.5	100 ("white light")	Kay & Grätzel 1993
TiO_2	A natural cyanin-dye	0.56	0.9	100 (AM1.5)	Cherepy et al. 1997

Costs of DSSC[7]

At the moment there is little information on the estimated costs for dye-sensitized solar cells available in the literature. And those that are given seem to vary significantly. Grätzel refers to a cost estimate commissioned from the Research Triangle Institute (USA) predicting a module cost of US $0.60/Wp.lxii Smestad et al. and Solaronix SA (Meyer 1996) have presented more detailed estimates for the manufacturing costs of DSSC modules. Both data are contrasted in Table 10

Smestad et al. 1994	US $/ m^2	Solaronix SA (Meyer 1996)[28]	US $/m^2
TiO_2 (10g/m^2)	0 03	Anatase screen printable paste	5.0
Ru-dye (100 mg/m^2 adsorbed)	7-10	Ru-dye	10.0
Pt catalyst (3 monolayers)	0 01	Pt catalyst	1.7
Electrolyte and iodide (50 ml/m^2)	0.1-1	Electrolyte and iodide salt	0.5
SnO_2:F Glass (10 Ω/sq)	30	SnO2:F Glass (10 Ω/sq)	30.0
Encapsulation and sealing	2-3	Sealant (primary + plugs)	3.0
Frame and electrical interconnections	2	Interconnect + contacts	5.0
Protective glass cover and Tedlar backing	2-3	Protective overcoats and connections	33.3
Materials subtotal	**43-49**	**Materials subtotal**	**88.6**
Production overhead	5-7	Rent floor space	0.9
Labor (100 people)	0.3-0.5	Labor (12 people)	13.2
Profit, Interest due top loans	0-8	Depreciation (20%)	8.0
Total module cost ($/m2)	**48-64**	**Total module cost ($/m2)**	**110.6**
Module efficiency	8-10 %	Module efficiency	5 %
Cost ($/Wp)	0.48-0.80		
Cost per W_p at 5% eff. ($/Wp)	**0.96-1.28**	**Cost ($/Wp)**	**2.2**

CHAPTER 6

Organic Solar Cells (OSC)

6.1 Introduction[10]

- Organic solar cells use polymers instead of metals or silicon to produce electricity from photons.
- Polymers are generally considered to be insulators, but a certain kind called conjugated polymers can transmit electrons with resistances very close to that of metals.
- Several of these electron donating polymers are known to photo luminance (a process in which an electron is promoted into the conduction band) when illuminated.
- In photovoltaic devices, donor polymers are paired with acceptor molecules. These acceptor molecules must be chosen such that the electrons in the conduction band are transferred from the donor molecule before they can relax from the excited state.
- Advantages of these solar cells is that they are relatively easy to produce on a manufacturing scale by methods like spin coating, dip coating, or a roll to roll process.

6.2 General Device Structures[10]

6.2.1 Bilayer Cells

- Bilayer organic photovoltaic cells are made by depositing donor and acceptor layers directly over one another.
- Only about 10% of the thickness of the contacting donor and acceptor layers will experience electron transfer.
- Thus, device efficiency is relatively low with this fabrication process.

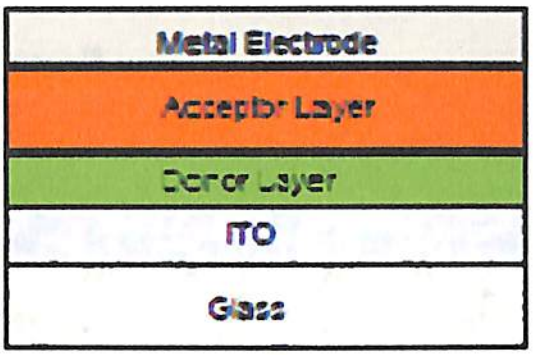


Fig. 20 : organic solar cell structure

6.2.2 Bulk Hetero junction Cells

- Similar to bilayer cells except the donor and acceptor are blended in a single layer.
- This design increases the surface contact between the donor and acceptor, significantly enhancing electron transfer, and increasing the efficiency compared to bilayer devices.
- Baytron is a dispersion of the conjugated polymer PEDOT and the polyanion, PSS.
- The Baytron layer smoothes out the electrode, helping to eliminate short

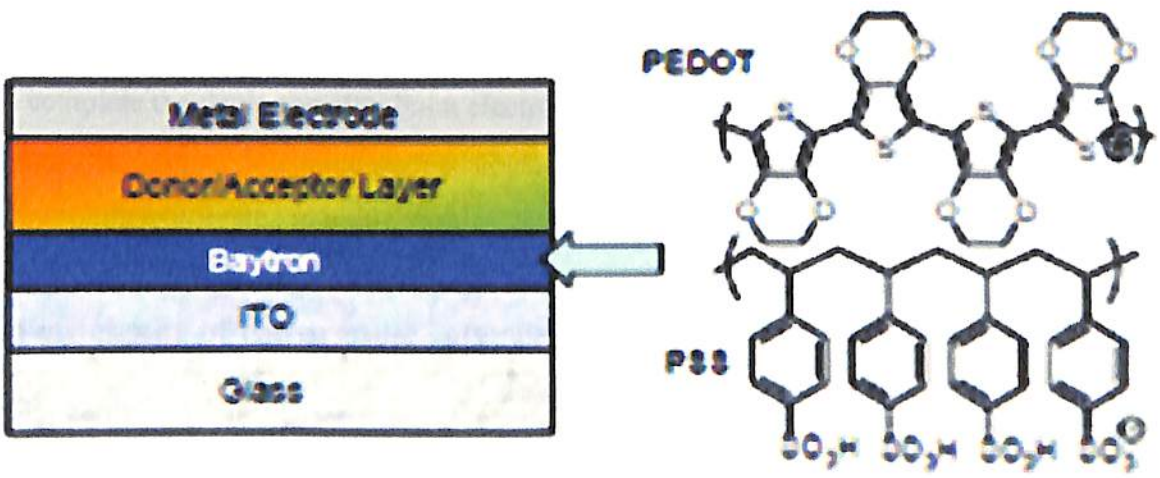


Fig.21: bulk hetero junction solar cell

6.3 Device Fabrication[10]

- Device performance has been shown to decrease rapidly when exposed to O_2 and H_2O.
- Thus, all processes involving the active polymer layer are done in a nitrogen environment glove box.

Fig.22: organic solar cell fabrication equipment

- While ITO is available commercially on glass slides, the Baytron and active polymer must be applied from solution.
- In this application, spin coating was used to produce a uniform film thickness from 50-200nm
- To complete the device an aluminum electrode must be applied.
- In order to achieve maximum surface contact with the active layer film the aluminum is thermally evaporated to a thickness of 100-200nm.

Cost and efficiency of the organic solar cell

Organic solar cell is 1/3 times cheaper than the inorganic solar cell. The efficiency of organic solar cell is approximately 3-4% which is very low in comparison to inorganic solar cell.

CHAPTER 7

Result

7.1 Comparison of various solar panel manufacturing technologies

Comparison of technologies including cost at various state, selling price and efficiency.

The following tables 11: give the efficiency and the cost of various solar module technologies

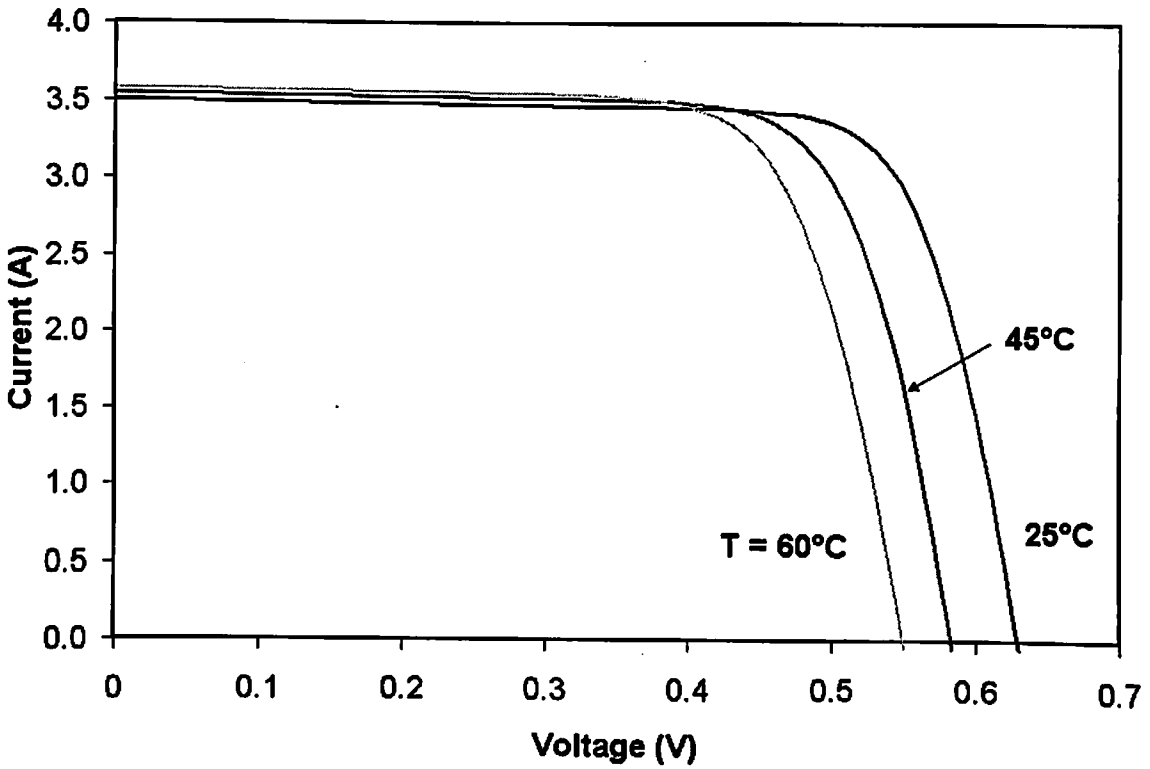
	12% Poly-Crystalline Si	6% a-Si	13% CIGS
Cost of Solar Cell Material	0.4	0.11	0.13
Cost of Solar Cell Labor	0.4	0.07	0.08
Cost of Module Material	0.25	0.37	0.17
Cost of Module Labor	0.5	0.07	0.08
Indirect Material	0.2	0.16	0.05
Energy Cost	0.3	0.06	0.04
Equipment Amortization	0.4	0.15	0.12
Manufacturing Overhead	0.1	0.1	0.06
Total Manufacturing Cost	2.55	1.09	0.73
Corporate Overhead (30%)	0.77	0.4	0.22
Total Cost	3.32	1.42	0.95
50% profit margin	1.66	0.71	0.47
Selling Price*	4.98	2.13	1.4

Table No.12: comparison of efficiency, area and weight of various companies using different technology

Company	Technology	Power Watt	Efficiency(η) %	Area	Weight (Kg)
Centre electronic limited(CEL)	Mono crystalline silicon	80	15.5	1200mm*550mm=0.66m^2	7.5
CEL	Mono crystalline silicon	160	15.9	1580mm*795mm=1.256 m^2	14
Moserbaer PV	Multi crystalline silicon	80	12	1206mm*540mm=0.651 m^2	9.5
XL tele com& energy limited	Multi crystalline silicon	175	13	1356mm*1001mm=1.36 m^2	16.8
Moserbaer PV	Amorphous thin film(a-Si)	105	6.1	1300mm*1100mm=1.43m^2	25
Powergen limited	CIGS	158	11.8	1909mm*874mm=1.66m^2	21.8

7.2 Effect of temperature on solar cell

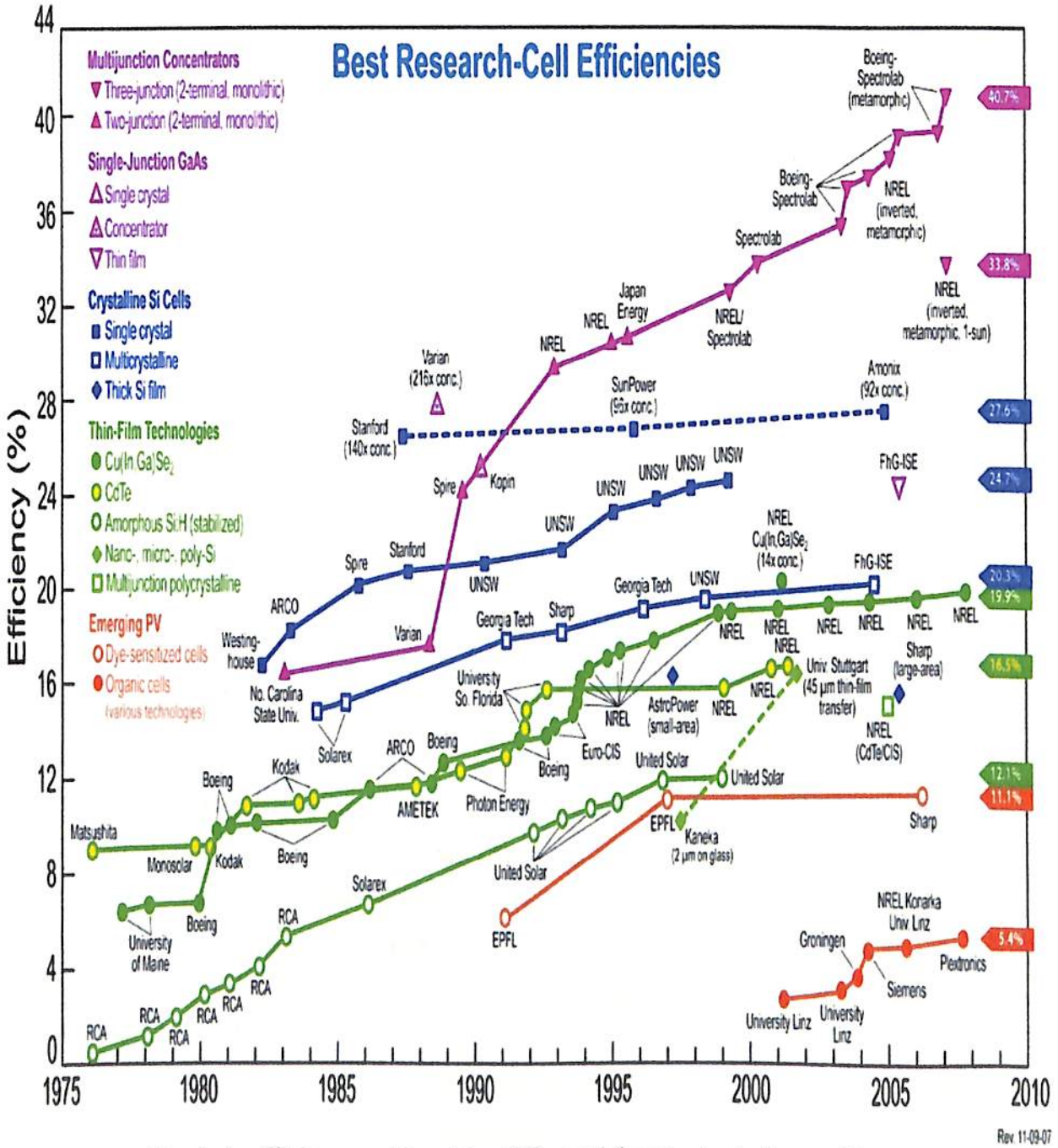
The overall effect of temperature on cell efficiency can be computed using these factors in combination with the characteristic equation. However, since the change in voltage is much stronger than the change in current, the cell voltage decreases by approximately 2.2mV per 0c rise in operating temperature, depending on the resistivity of the silicon used: higher the silicon resistivity more marked temperature effect the overall effect on efficiency tends to be similar to that on voltage. Most crystalline silicon solar cells decline in efficiency by 0.50%/°C and most amorphous cells decline by 0.15-0.25%/°C. The graph shows I-V curves that might typically be seen for a crystalline silicon solar cell at various temperatures.



Graph 3: effect of temperature V and I curve

7.3 Solar cell efficiency achieved by the various laboratories in the world.

The graph 4: given below provides the solar cell efficiency achieved by the various laboratories in the world.



Graph 4: efficiency achieved by different laboratories in the world

Graph 4: efficiency achieved by different laboratories in the world

Conclusion

The PV industry is growing rapidly (~35%/yr) due to improvements in the efficiency and cost of silicon solar cells and the demand for alternative energy resources. Currently, 85% of the PV modules produced are made of crystalline Si. Silicon base wafer technologies benefit from the established infrastructure of Si and the large plant capacities. The increased production volume has also led to a reduction in the module cost However, in the future, the dominance of traditional silicon technologies will diminish as thin film technologies mature. Thin films offer a new generation of high power, low cost, and relatively environmentally benign solar cells. In addition, some advantageous properties of thin- film PV relative to wafer-based PV include monolithic design leading to reduced parts handling, low consumption of both direct and indirect materials, and fewer process steps. In the past 20 years, the advancement of solar cells has seen a dramatic rise in the efficiencies of the modules. some of the thin film technologies are beginning to approach the efficiencies of crystalline silicon. In addition, many of the thin film technologies can be incorporated onto light-weight and flexible substrates, which can be adapted to almost any shape and therefore can be used in numerous applications. However, a balance between low cost and high efficiency has yet to be achieved. Compound semiconductors (CdTe, CIGS) offer the possibility of high efficiencies but are currently difficult to process and the extent of their use will be ultimately determined by the scarcity of their core materials. CIGS, the most efficient of the thin films developed thus far, probably will suffer from the limited quantities of In. The major problem of CdTe solar cells is the toxicity of the Cd component, which can have a significant environmental impact if released. In fact, the potential health and environmental impacts of Cd are so great that they have caused many groups to shy away from any Cd-based technology hindering its further development Thin film silicon offers a promising alternative, since they combine the already established infrastructure of silicon and the beneficial properties of thin film technologies.

Currently, this technology is in its infancy as far as development is concerned, although exotic processing may be required. Amorphous Si is much cheaper to produce than crystalline Si using roll- to-roll manufacturing but suffers from low efficiencies.

Unfortunately, low deposition rates in the roll- to-roll processing and the required high quality TCO layers have limited the optimization of the manufacturing process. This has caused the price of a-Si
modules to be only marginally lower than their crystalline counterparts but changes in materials and processing could make a-Si more economically favorable but the efficiency is decreased in this technology.

Dye sensitized and organic solar cells are in the early stage of development, although the possibility of inexpensive roll-to-roll manufacturing, similar to other thin film cells, makes the prospects exciting. These technologies also benefit from a short energy payback time. One of the main drawbacks of the technology at the current moment is the high material costs, however these costs may be reduced in large scale production formats. Improvements in efficiency and lifetime are also required to allow for large scale commercialization. We have evaluated the most prominent technologies in comparison with each other to assess their relative advantages and disadvantages. We conclude that each technology has promising potential and important barriers that they will need to overcome.

However, they are probably best viewed not as mutually exclusive possibilities, but as devices that are likely to become adopted in different applications, at different stages, and possibly in new combinations with each other. For example, thin films may find opportunities in applications where power density (W/m^2) is not important, but cost and weight are. Because these technologies are at different stages in development, they are likely to emerge at different
times. So, based on above study it could be inferred that in the near future, crystal silicon will continue to dominate (5-10 years) while the alternative thin film technologies (CIGS, CdTe, a-Si) beginning to supplant bulk crystalline devices in the intermediate future. Barring significant new material breakthroughs or barriers in development, thin film Si and organic based cells have a chance to have a dominant market share in the long term future. Due to the expected continued growth of the photovoltaic industry, the dominant technologies of the future will be those that best adapt to the changing market needs.

References

1. *Non conventional energy resources written by BH Khan TMH publication*
2. *Handbook of Photovoltaic Science and Engineering Edited by Antonio Luque Instituto de Energ'ıa Solar, Universidad Polit'ecnica de Madrid, Spain and Steven Hegedus Institute of Energy Conversion, University of Delaware, USA*
3. *www.green-plnet-solar-energy*
4. *Centre electronic limited Sahibabd (U.P.) http://www.celindia.co.in*
5. *USL photovoltaic limited Coimbatore www.uslpv.com*
6. *Moserbaer PV technology limited Noida(U.P.) http://www.moserbaerpv.in*
7. *Photovoltaic Technology Review Andy Baumann, Yash Bhargava, Z.X. Liu, Gregory Nemet, James WilcoxMSE/C226 December 6, 2004*
8. *www.ezinearticle.com/expert=kriss Bergethon*
9. *Powergen limited Mumbai www.powerzenonline.com*
10. *Organic Solar Cells from Functionalized Donor-Acceptor Molecules by Colin W. Gurganus, AFRL/MLBP, Wright-Patterson Air Force Base Michael F. Durstock, Rachel R. Smith, Adam P. Smith, Barney E. Taylor, Long Y. Chiang U.S.A.*