Enrolment No:	UPES UNIVERSITY WITH A PURPOSE

UNIVERSITY OF PETROLEUM AND ENERGY STUDIES
End Semester Examination, July 2020

Course: DIGITAL ELECTRONICS **Semester: IV**
Program: B.Tech Electrical Engineering **Time 03 hrs.**
Course Code: ECEG 2016 **Max. Marks: 100**

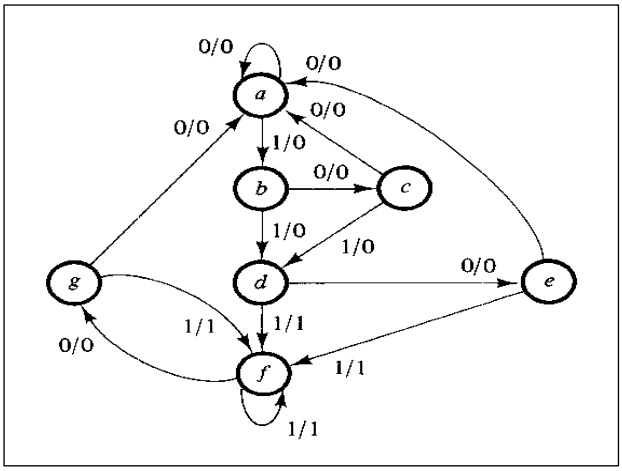
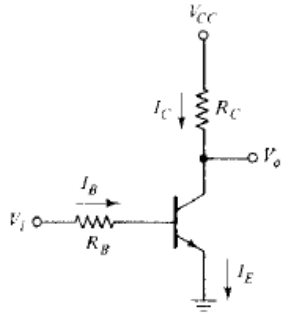
Instructions:

1. **Attempt all the questions (Theory, Numerical, Case study etc.) on A4 size blank sheets.**
2. **Attempt all questions serially as per question paper.**
3. **Answer should be neat and clean. Draw a free hand sketch for circuits/tables/schematics wherever required.**
4. **Scan the whole answer script and check the resolution carefully before upload on the blackboard. Note that answer scripts will be considered for evaluation only through Blackboard. No other mode of submission is acceptable.**
5. **You are expected to be honest about each attempt which you make to progress in life**

SECTION A [Case Based Study/design] 40 Marks

S. No.		Marks	CO
1.	Design a Seven segment display decoder for the (i) numbers 0-9 (ii) for 10 as 'A' (iii) for 11 as 'B' (iv) for 12 as 'C' (v) for 13 as 'D' (vi) for 14 as 'E' (vii) for 15 as 'F'	**20**	**CO5**
2.	a)Implement the following Boolean functions using PAL with four inputs with AND- OR structure. $F_1(A,B,C,D)=\Sigma m(2,12,13)$ $F_2(A,B,C,D)=\Sigma m(7\text{-}15)$ $F_3(A,B,C,D)=\Sigma m(0,2\text{-}8,10,11,15)$ $F_4(A,B,C,D)=\Sigma m(1,2,8,12,13)$ b)Design a PLA circuit to implement the 3-bit binary to Gray code conversion.	**15+5**	**CO 5 & CO 4**

NOTE : The submission time of the Question Paper Answer Sheet is 24 Hhrs from the scheduled time (*exceptional provision due to extraordinary circumstance due to COVID-19 and due to internet connectivity issues in the far-flung areas*).
No Submission will be entertained after 24 Hrs

SECTION B [Numerical and Short/broad Answers] 60 Marks			
3.	a)Reduce the number of Flip Flops required for the below state diagram Fig 1  **Fig 1** **[or]** b)For the circuit shown below in the figure 2 , the R_C=1kΩ, R_B=22kΩ, h_{FE}=50, logic high value is 5Vand logic low L=0.2 V. Show that it is an inverter circuit not an amplifier  **Fig 2**	**10**	**CO4**
4.	Reduce the following function using six variable K- map $F = \Sigma m(0, 2, 5, 7, 9, 11, 14, 16, 18, 21, 23, 27, 30, 32, 34, 36, 41, 43, 44, 48, 50, 52, 53, 59, 60, 61)$.	**10**	**CO 2**
5.	Design a MOD-10 synchronous counter using T flip-flops.	**10**	**CO 3**

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6.	Explain about the (i)Edge triggering (ii) Master Slave Flip Flop (iii)Race Around (iv) Indeterminate state (v)Noise Margin in Logic circuits	**5**	**CO1**
7.	Design a multiplexer circuit which implements the function $F_1(A,B,C,D,E)=\Sigma m(0, 2, 5, 7, 9, 11,12,13, 17,19, 22,28, 29,)$	**10**	**CO2**
8.	(i)Design of R-2R ladder D/A Converter for four bit binary number conversion into analog equivalent (ii)A 4 bit R-2R ladder type D/A Converter having resistor values of R=10kΩ and 2R=20kΩ uses V_R of 10 V. Find (i)the resolution of the D/A Converter, (ii)for a digital input of 1011.	**5** **10**	**CO 4**

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