Name: **Enrolment No:**	UPES

UNIVERSITY OF PETROLEUM AND ENERGY STUDIES

End Semester Examination, July 2020

Programme Name: B. Tech- Fire Safety Engineering **Semester : II**
Course Name : Basic Electronics Engineering **Time : 03 Hrs.**
Course Code : ECEG-1002 **Max. Marks: 100**
Nos. of page(s) : 3

Instructions:

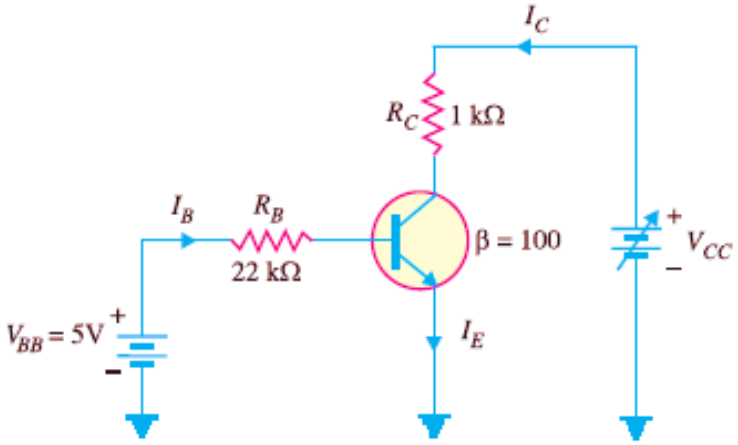
1. **Attempt all the questions (Theory, Numerical, Case study etc.) on A4 size blank sheets.**
2. **Attempt all questions serially as per question paper.**
3. **Answer should be neat and clean. Draw a free hand sketch for circuits/tables/schematics wherever required.**
4. **Scan the whole answer script and check the resolution carefully before upload on the blackboard. Note that answer scripts will be considered for evaluation only through Blackboard. No other mode of submission is acceptable.**
5. **You are expected to be honest about each attempt which you make to progress in life.**

SECTION- A [Case Based Study/design] 40 Marks

S. No.	Attempt all the questions. Assume data, if not given.	Marks	CO
Q 1	An interactive learning is best tool from primary education to graduate engineering level always. For the outcome based education (OBE), a system is required to design engineering students with the help of basic logic gates. Required information is given to design basic logic gate based daigram (cobmnational circuit) as, "Proposed system that accepts a 3-bit BCD numbers and geneartes an ouput binary number equal to the addition of the input number".	**20**	**CO3**
Q 2	It is well known that if high ripple factors existed in the DC supply is unacceptable for an electronics device. **(i)** What you will do for removing these undesirable ripples from the voltage supply. Analyze the operation of any two methods with circuit diagram design and required output waveform. **(ii)** Show the significance of filter circuits and importance of voltage regular to design a single circuit diagram for delivering power supply +5V and +9V DC output separately.	**20**	**CO1**

SECTION-B [Numerical and Short/broad Answers] 60 Marks

NOTE : The submission time of the Question Paper Answer Sheet is 24 Hhrs from the scheduled time (*exceptional provision due to extraordinary circumstance due to COVID-19 and due to internet connectivity issues in the far-flung areas*).
No Submission will be entertained after 24 Hrs

Q 3	Design a logic gate circuit diagram (Combinational circuit), which having output '1' (HIGH) when a 4-bit hexadecimal input is an odd number from 0 to 9.	**7**	**CO3**
Q 4	The transistor shown in Fig (1) has the following assumptions: $P_{D(max)}$ =800 mW, $V_{CE(max)}$ =15V, $I_{C(max)}$=100 mA. Determine the maximum value to which V_{CC} can be adjusted without exceeding any rating. Which rating would be exceeded first?  Fig. (1)	**10**	**CO2**
Q 5	Defend the resistivity of depletion layer of PN junction during the forward and reverse bias conditions. Also sketch the V-I characteristic with important notations.	**5**	**CO1**
Q 6	Convert the following numbers into corresponding number system **a.** $(306.12)_{10} = (?)_{16}$ **b.** $(101011.11)_8 = (?)_{10}$ **c.** $(63)_{10} = (?)_8$ **d.** $(001011100010100)_2 = (?)_{16}$ **OR** Design and Full adder logic circuit diagram using two Half adders. Also draw the block diagram with truth table.	**8**	**CO3**
Q 7	A semiconductor diode having ideal forward and reverse characteristics is used in half wave rectifier circuit supplying a resistive load of 1000Ω. If the r.m.s. value of the supply voltage is 250V, determine (i) the r.m.s. diode current (ii) power dissipated in the load.	**10**	**CO1**
Q 8	Explain the electrical equivalent circuit of PN junction diode. Differentiate the Approximate and simplified diode model.	**5**	**CO1**

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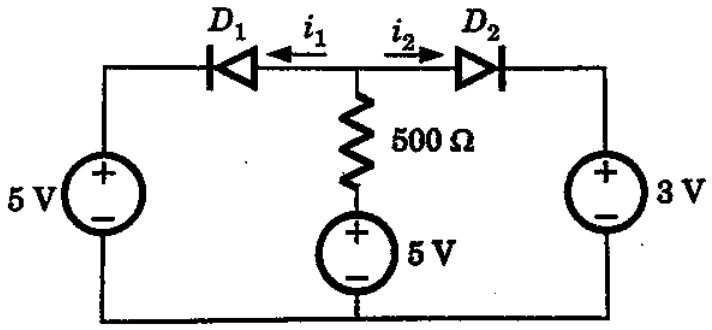
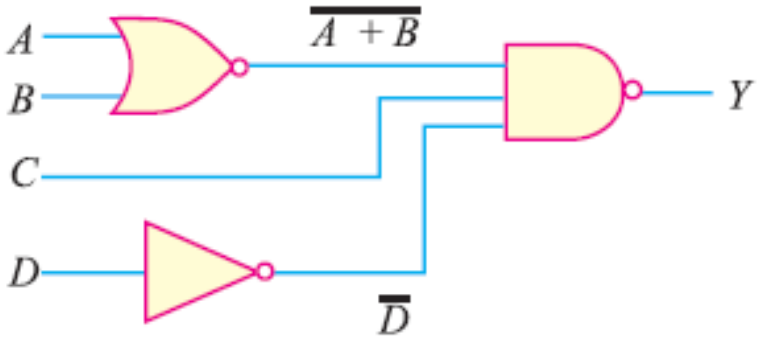
Q 9	In the circuit of Fig. (2), Diodes D_1 and D_2 are ideal diodes. Determine the current I_1 and I_2.  **Fig. (2)**	**5**	**CO2**
Q 10	Simplify the following function using K-map and realize the obtained (simplified) function using NAND universal Logic Gate. $F(A,B,C,D)= \sum (0,3,5,7,8,9,10,12,15)$. **OR** Determine the output expression for the given circuit shown below in Figure (3). (i) Simplify it using De Morgan's theorem (ii) realize the simplified expression using NAND universal Logic Gate.  **Fig. (3)**	**10**	**CO3**

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