

Name:
Enrolment No:



UNIVERSITY OF PETROLEUM AND ENERGY STUDIES

End Semester Examination, July, 2020

Programme Name: **B. Tech- CSE-All** Semester : **VI**
Course Name : **Microprocessor & Embedded Systems** Time : **03 hrs**
Course Code : **CSEG 3006** Max. Marks: **100**
Nos. of page(s) : **16**
Instructions: **Assume any data in programming, if required**

Note: **Common to B. Tech- CSE All, 6th Sem (CCVT, IT-Infra, Mainframe, Cyber Law + IPR, Big Data, Dev Operations, CSF (Cyber Security and Forensics), Graphic & Gaming, Open System Standard, CSF, BAO , BFSI)**

Quiz Based Examination

Q 1. _____ ports allow data flow between microcontroller and other devices such as PC or other microcontroller. Point: 2

- a) GPI
- b) interrupts
- c) **Serial put/output ports**
- d) All of the above

Q 2. The SP of 8051 controller is _____ bits wide register. And this may be defined anywhere in the _____. Point: 2

- a) "8 byte, on-chip 128 byte RAM. "
- b) "16 bit, on chip 256 byte RAM. "
- c) **"16 bit, on-chip 128 byte ROM "**
- d) "8 bit, on chip 128 byte RAM."

Q 3. The size of internal RAM memory of the 8051 is: Point: 1

- a) 128 bits
- b) 128KB
- c) 128MB
- d) **128 bytes**

Q 4. For implementing concept of pipelining 8051 controller should have.....memory architecture. Point: 1

- a) Non-multiplexed
- b) Multiplexed
- c) Von-Neumann Architecture
- d) **Harvard Architecture**

Q 5. What is the use of Auxiliary carry flag? Point: 1

- a) **BCD addition**
- b) BCD subtraction
- c) BCD Multiplication

d) All of the above

Q 6. 8051 PSW is also called as

Point: 1

- a) **Flag Register**
- b) 91H & 97H
- c) 91H & 91H
- d) 97H & 97H

Q 7. Number of banks and number of registers each bank of 8051 controller respectively are Point-2

- a) 4 and 32
- b) 4 and 4
- c) 4 and 16
- d) **4 and 8**

Q 8. The length of address bus of 8051 is of ___ bytes?

Point: 1

- a) 16
- b) 8
- c) 4
- d) 2

Q 9. Data transfer from I/O to external data memory can only be done with the _____ command.

Point: 1

- a) **MOVX**
- b) MOVC
- c) MOVXC
- d) MOV CX

Q 10. To fetch address of next instruction 8051 will do a _____

Point: 1

- a) Write operation from program counter
- b) 000FH Read and write operation from program counter
- c) **Read operation from program counter**
- d) None of the above

Q 11. "What is the value of carry flag and auxiliary carry flag after the end of following program:

CLR C MOV A, #3FH

Point: 1

MOV R3, #23H

ADD A,R3 "

- a) "CY=1,AC=0"
- b) "CY=0,AC=0"
- c) "CY=1,AC=1"
- d) **"CY=0,AC=1"**

Q 12. "The content of B register after execution of following instructions:

Point: 1

MOV A, # 74

MOV B, #10

DIV AB

MUL AB"

- a) **B=04**
- b) B=03
- c) B=02
- d) B=05

Q 13. "What is the content of register A after the execution of following instructions: Point: 1

MOV A, #45H

XRL A, #54H

- a) 15H
- b) **11H**
- c) 20H
- d) 2CH

Q 14. "P1.2. is used to control an outdoor light and P1.5 is used to control the light side the building
SETB C ORL C, P1.2 MOV P1.2,C CLR C ANL C,P1.5 MOV P1.5,C" point: 2

- a) Both Lights Off
- b) Both Lights On
- c) **Outdoor Light ON and side Light OFF**
- d) Outdoor Light OFF and side Light ON

Q 15. "Find the content of register A after the following instruction is executed: Point: 1

MOV A,#56H SWAP A RR A RR A"

- a) 52H
- b) **59H**
- c) 62H
- d) 65H

Q 16. "CJNE A, data means _____" Point: 1

- a) **Jump if A is not equal to data**
- b) Jump if A is equal to data
- c) Jump and decrement A
- d) Jump and increment A

Q 17. "Find how many times the loop will run? MOV A,#55H MOV R3,#10H Point: 1

NEXT: MOV R2,#70H AGA: CPL A DJNZ R2,AGA DJNZ R3, NEXT"

- a) 70
- b) **700**
- c) 699
- d) 701

Q 18. "Find the content of register R1 after the execution of following program:

Point: 1

CLR C MOV A,#02H ADDC A,#0FCH MOV R1, A"

- a) FDH
- b) FEH
- c) **FFH**
- d) FBH

Q 19. "Find out the content of PSW after the execution of the following instruction. Point: 1

MOV A, #0BFH ADD A,#1BH"

- a) **41H**
- b) 51H
- c) 45H
- d) 54H

Q 20. "Find the content of register A after the following instruction is executed: Point: 1

CLR A ORL A, #99H CPL A"

- a) 33H
- b) **66H**
- c) 55H
- d) 44H

Q 21. 8051 C programming what is the significance of for(;;) instruction Point: 1

- a) infinite loop
- b) **infinite loop**
- c) Loop will run 1000 times
- d) None of These

Q 22. 8051 C programming the magnitude of the number ranges from? Point: 1

- a) 0 to 255
- b) **-32768 to 32767**
- c) 0 to 65535
- d) -128 to 127

Q 23. 8051 C programming what is the output at PO port after the execution of following instruction? Point: 1

P0=0X6<<3

- a) **03H**
- b) 0CH
- c) 09H
- d) 05H

Q 24. " 8051 C programming if LED is connected at P1 port then how many times it will glow (count range)? Point: 2

```
#include <reg51.h>      void ma(void) {      P1=00H      for(;;) {  
P1++;      }      }
```

- a) **count from 00 to FFH**

- b) count from 00 to 10H
- c) count from 00 to 55H
- d) count from 00 to 20H

Q 25. What is the output of the following instruction? P1=0X54H^0X78H Point: 1

- a) 20H
- b) **2CH**
- c) 24H
- d) 26H

Q26. In LCD RS Pin is an _____ pin Point: 1

- a) **input**
- b) Output
- c) Both put and output
- d) None of These

Q 27. "Identify the row and column of the pressed key 4X4 Keyboard D3-D0=1110 for the row, D3-D0=1011 for the column" Point: 1

- a) Key 9
- b) **Key 2**
- c) Key 5
- d) Key 9

Q 28. " LED interfacing if 8 LEDs are connected to P1 port, then for blkg alternate LED what hexcode should be sent to port P1?" Point: 1

- a) **AAH**
- b) 81H
- c) 42H
- d) 24H

Q 29. Seven display which hexcode should be sent to display number 2 at the output Point: 1

- a) BFH
- b) 86H
- c) **DBH**
- d) EFH

Q 30. Which of the following is one of the type of analog to digital converter? Point: 1

- a) R/2R Ladder Network
- b) **Successive Approximation**
- c) Binary weighted
- d) None of These

Q 31. " 8085 microprocessor, how many interrupts are maskable." Point: 1

- a) Two
- b) Five
- c) three
- d) **Four**

Q 32. The instruction RET executes with the following series of machine cycle Point: 1

- a) **"Fetch, read, read"**
- b) "Fetch, read, write"
- c) "write, read, fetch"
- d) "Fetch, read"

Q 33. "If the interrupt is to be vectored to any memory location then which of the above interrupt is/are ? Point: 1

1 . TR

2. RST 5.5

3. RST 6.5

4. RST 7.5

5. TRAP"

- a) 1 and 2 only
- b) **1 only**
- c) "1, 2, 3 and 4"
- d) 5 only

Q 34. "Consider the following statements: Point: 1

1. Auxiliary carry flag is used only by the DAA and DAS instruction.

2. Zero flag is set to 1 if the two operands compared are equal.

3. All conditional jumps are long type jumps."

- a) 1 and 3 only
- b) "1, 2 and 3 only"
- c) **1 and 2 only**
- d) 2 and 3 only

Q 35. " 8085 microprocessor, the address for 'TRAP' interrupt is" Point: 1

- a) 002C H
- b) **0024 H**
- c) 0034 H
- d) 003C H

Q 36. " 8085, the RST instruction will cause an interrupt _____." Point: 1

- a) **every time it's executed**
- b) only if interrupts have been enabled by the EI (Enable interrupt) instruction
- c) only if the interrupt mask bit is set to 0
- d) only if an ISR is not actively executing

Q 37. "What will be the value the memory location 7101H after the execution of the following code?
The data at memory location 7100 is A7H. Point: 2

LXI H,7100H

MOV A, M

CMA

R A

STA 7101H

HLT"

- a) 58H
- b) **59H**
- c) 5AH
- d) none of these

Q 38. The 8085 microprocessor enters to bus idle machine cycle whenever Point: 1

- a) TR interrupt is recognized
- b) DAD RP instruction is executed
- c) **RST 7.5 is recognized**
- d) none of these

Q 39. "How many times NOP instruction will be executed the following program; MVI A, 10H

MVI B, 10H Point: 1

BACK: NOP

ADD B

RLC

JNC BACK

HLT"

- a) 3
- b) 2
- c) 10
- d) 4

Q 40. "What is the content of A-Register at the end of this program? Point: 1

XRA A

MVI B, F0H

SUB B "

- a) 0FH
- b) **10H**
- c) F0H
- d) 0EH

Q 41. "What is the content of A at the end of this program? Point: 1

STC

MVI A, 35H
ACI 26H "

- a) C5H
- b) **5CH**
- c) CCH
- d) 55H

Q 42. "What is the content of A at the end of this program?"

Point: 1

MVI A, 06H

RLC

MOV B, A

RLC

RLC

ADD B "

- a) 18H
- b) **3Ch**
- c) C2H
- d) 22H

Q 43. "What is the status of z flag, cy flag, sign flag at the end of this program?"

Point: 1

MVI A, 02H

MVI B, 03H

ADD B

XRA A "

- a) **"1,0,0 "**
- b) "0,1,0 "
- c) "1,0,0 "
- d) "1,0,1"

Q 44. "What is the content of Register A at the end?"

Point: 1

XRA A

MVI B, 4DH

SUI 4FH

ANA B

HLT"

- a) **01h**
- b) 0DH
- c) 00H

d) 10H

Q 45. "Calculate the total delay for the given set of instructions (internal clock frequency is 3MHz)

MVI B,FFH

Point: 2

LOOP: DCR B

JNZ LOOP

RET"

- a) 1400 μ s.
- b) **1194.66 μ s.**
- c) 1400.66 μ s.
- d) 1440 μ s.

Q 46. "Calculate the total delay for the given set of instructions (internal clock frequency is 6 MHz)

MVI B,FFH

Point: 2

L1: MVI C,FFH

L2: DCR C

JNZ L2

DCR B

JNZ L1

RET"

- a) **152.5 μ s.**
- b) 305 μ s.
- c) 102.5 μ s.
- d) 752.5 μ s.

Q 47. "Calculate the total delay for the given set of instructions (internal clock frequency is 3 MHz)

LXI B,FFFFH

Point: 1

LOOP: DCX B

MOV A,B

ORA C

JNZ LOOP

RET"

- a) 1.52428s
- b) **0.52428s**
- c) 2.34 μ s.
- d) 6.34 μ s.

Q 48. "Consider the following statements:

Point: 1

1. Auxiliary carry flag is used only by the DAA and DAS instruction.

2. Zero flag is set to 1 if the two operands compared are equal.

3. All conditional jumps are long type jumps"

- a) **1 and 2 only**
- b) "1, 2 and 3 only"
- c) 1 and 3 only
- d) 2 and 3 only

Q 49. A 'DAD H' instruction is the same as shifting each bit by one position to the right with a zero inserted Point: 1

- a) LSB position
- b) left
- c) **left with a zero inserted LSB position**
- d) right

Q 50. What type of instructions can potentially change the sequence of operations a program?

Point: 1

- a) Logical instructions
- b) **Branch instructions**
- c) Data transfer instructions
- d) Arithmetic instructions

Q 51. _____ is defined as a combination of letters to suggest the operation of an instruction.

Point: 1

- a) **Mnemonic**
- b) Opcode
- c) Byte
- e) None of these

Q 52. For a data transfer operation

Point: 1

- a) contents of Source are destroyed & of destination are changed
- b) Source are destroyed & of destination are not changed
- c) **Source are not destroyed & of destination are changed**
- d) Source are not destroyed & of destination are not changed

Q 53. _____ instruction/s can alter the sequence of a program either by calling/returning subroute or when a condition is met. Point: 1

- a) Return
- b) Call
- c) Jump
- d) **All of the above**

Q 54. To communicate with memory the microprocessor unit should be able to

Point: 1

- a) Select the chip
- b) Identify Register
- c) R/W from or to register

d) **All of the above**

Q 55. The number of address lines required for 8K memory chip are _____. Point: 1

- a) **13**
- b) 12
- c) 11
- d) 14

Q56. "If the content of register A & B is FFH and 98H respectively, determine the content of accumulator & flag register after executing ADD B instruction." Point: 1

- a) **97H & 91H**
- b) 91H & 97H
- c) 91H & 91H
- d) 97H & 97H

Q 57. The 8085 can respond to following externally initiated operations Point: 1

- a) Reset
- b) Hold
- c) interrupt
- d) **All of the above**

Q 58. Devices used for interconnecting peripherals with 8085 include _____. Point: 1

- a) Buffers
- b) Decoder/Encoder
- c) Latches
- d) **All of the above**

Q 59. The status of _____ indicates data conditions after an ALU operation 8085. Point: 1

- a) **Flag Register**
- b) instruction Register
- c) Stack Pointer
- d) None of the above

Q 60. For an 8K byte memory if the address of last location is FFFFH then the starting address is _____. Point: 1

- a) 0000H
- b) 000FH
- c) **E000H**
- d) F000H

Q 61. "The instruction MOV B,M copies the contents of memory location register B. It is a 1 byte instruction with two machine cycles and seven T-states. The second machine cycle and its control signal are" Point: 1

- a) **Memory Read; RD'**
- b) Memory Write ; WR'
- c) I/O Write ; WR'
- d) I/O Read; RD'

Q 62. "If the clock frequency is 5MHz, then how much time is required to execute an instruction of 18-T states?" Point: 1

- a) 5.2 μ s
- b) 1.8 μ s
- c) **3.6 μ s**
- d) 3 μ s

Q 63. The _____ signal helps differentiating between put and output ports of same address 8085. Point: 1

- a) Timing
- b) **Control**
- c) Status
- d) None of the above

Q 64. The data bus 8085 is _____ . Point: 1

- a) **bi-directional**
- b) partially unidirectional & partially bi-directional
- c) unidirectional
- d) None of the above

Q 65. The sequence of instruction execution 8085 is performed by _____ Point: 1

- a) **Program Counter**
- b) Stack Pointer
- c) instruction Register
- d) Accumulator

Q 66. Which of the following is/are sync pulses indicating availability of data on the data bus?

Point: 1

- a) RD'
- b) WR'
- c) **Both a. & b**
- d) None of the above

Q 67. "Assume that the accumulator contains data byte 82H, and the instruction MOVCA (4FH) is fetched. What is the first step decoding and executing the instruction 8085?" Point: 1

- a) Transfer the content of temporary register to register C.
- b) Transfer the contents of A to temporary register ALU.
- c) **Place the content of data bus (4FH) the instruction register and decode instruction**
- d) None of the above

Q 68. "Identify IO/M', RD' and WR' as status or control signals respectively. (Consider same sequence)" Point: 2

- a) "Status,Control,Status"
- b) "Control, Status,Control"
- c) "Control, Status,Status"
- d) **"Status, Control, Control"**

Q 69. "Mostly opcode fetch, memory read and memory write cycles consist of ____, ____ & ____ T-states respectively." Point: 1

- a) **"4,3,3"**
- b) "3,4,4"
- c) "3,4,3"
- d) "4,3,4"

Q 70. For which of the following 8085 instruction flag register is affected? Point: 1

- a) IN
- b) INX
- c) **INR**
- d) DCX

Q 71. Which pin of the LCD is used for adjusting its contrast? Point: 1

- a) VCC
- b) R/W
- c) **VEE**
- d) RS

Q 72. "The following Five instructions are executed on 8085 Microprocessor : The result of accumulator after last instruction is MVI A, 33H ; MVI B, 78 H; ADD B; CMA; ANI 32 H"

Point: 2

- a) 00 H
- b) **10 H**
- c) 11 H
- d) 32 H

Q 73. For a RTOS system the interrupt latency should be Point: 1

- a) **less**
- b) more
- c) equal
- d) unequal

Q 74. The function of the personal computer using a user is an example of Point: 1

- a) Hard Real time system
- b) **Soft real time system**
- c) Uncoded Real time system
- d) None

Q 75. Which is not a tool for RTOS Point: 1

- a) Vx works
- b) Free scale Max
- c) Keil
- d) **Quatus-2 For NIOS-II**

Q 76. The STA 2003H instruction in 8085 microprocessor takes Point: 1

- a) 7 Tstate
- b) 10 Tstates
- c) **13T states**
- d) 16 T states

Q 77. LDA 2050 instruction in 8085 Microprocessor is an example of Point: 1

- a) **Direct addressing**
- b) direct addressing
- c) Implied addressing
- d) Immediate addressing

Q 78. Which is not the state of a task in RTOS Point: 1

- a) Ready
- b) Running
- c) Dormant
- d) **Kernel**

Q 79. Who is the core of the operating system which is responsible for management of the task Point: 1

- a) **Kernel**
- b) Dispatcher
- c) BIOS
- d) None of above

Q 80. Which is not an example of Semaphore Point: 1

- a) Binary
- b) Counting
- c) Mutex
- d) **Kernel**

Q 81. Which is not an example of Scheduling in RTOS Point: 1

- a) Pre-emptive scheduling
- b) Non preemptive Scheduling
- c) Round Rob Scheduling
- d) Deadlock

Q 82. Which instruction is used for indexed addressing in 8051 microcontroller Point: 1

- a) MOV
- b) MOV X
- c) MOV @RI
- d) **"MOV A, @ A+DPTR"**

Q 83. Which IC is used to interface the 8051 microcontroller to a DC motor Point: 1

- a) LM 35
- b) LC 28
- c) **L293D**
- d) MAX 232

Q 84. Asynchronous Communication the start bit is always Point: 1

- a) **0 (Logic Low)**
- b) 1 (logic high)
- c) d (don't care)
- d) x(undetermined)

Q 85. The microprocessor ask each device a sequence where it is ready for communication or data transfer. The technique called is Point: 1

- a) **polling**
- b) interrupt
- c) Task management
- d) Synchronization

Q 86. "The 8085 microprocessor has the data A= 10101010, After rotating the data two times, the output will" Point: 1

- a) 1111
- b) 11110000
- c) **10101010**
- d) 1010101

Q 87. If the clock frequency of 8085 microprocessor is 3 MHZ. Then the time period for the instruction JNZ 10T- state will be Point: 1

- a) 5 microsecond
- b) **3.3 microsecond**
- c) 10 microsecond
- d) 3 microsecond

Q 88. How many memory chips are required to configure a (4KX8) memory size using (256 x 8) RAM chip Point: 1

- a) 4
- b) **16**
- c) 32
- d) 64

Q 89. The high level language program is converted to machine language Point: 1

- a) Assembler
- b) **Compiler**
- c) Cross compiler
- d) Linker

Q 90. Which instruction is used to add 16-bit number 8085 microprocessor Point: 1

- a) ADD
- b) ADC
- c) **DAD**
- d) SUB

