Name:

Enrolment No:



UNIVERSITY OF PETROLEUM AND ENERGY STUDIES

End Semester Examination, December 2019

Course: Computer Organization and Architecture

Semester: 3rd Program: BCA Time: 03 hrs.

Course Code: CSEG 2014 Max. Marks: 100

Instructions: All questions of section A are compulsory. Question number 9 (Section B) and 11 (Section C)

have internal choice.

Q 1.		Marks	CO
	Describe auxiliary memory in brief.	4	CO
Q 2.	Describe the typicality of Von Neumann's architecture with appropriate diagram.	4	CO
Q 3.	Write a short note on bus interface.	4	CO
Q 4.	Explain in brief, the idea of superscalar processing.	4	CO
Q 5.	Draw the circuit diagram and Truth table of a 8x3 encoder.	4	CO
	SECTION B		
Q 6.	Describe with the help of flow chart, the working of the flags FGI and FGO in the process of I/O.	10	CO2
Q 7.	With the help of necessary diagram, design the control unit of a basic computer that has 4Kof main memory and 16 bit shared bus. Give necessary explanations, where necessary.	10	CO
Q 8.	What is the importance of the flag IEN? Which is the flag that indicates if the CPU is in interrupt cycle or instruction cycle? Explain the structure of instruction resister along with diagram.	2+2+6	CO2
Q 9.	(a) With the help of necessary diagram, discuss the direct and indirect mode of memory access. What is bus arbitration? OR	8+2	CO2
	b) List and explain the steps involved in the execution of the instruction D4: SC — 0 along with flow chart and timing diagram.	10	CO2

	SECTION-C		
Q 10.	(a) Design 4-bit adder/Subtractor (with carry) and explain its function.(b) Describe with necessary diagram the working of interrupt controlled I/O.	10+10	CO1, CO3
Q 11.	 (a) What are micro operations? Write down the micro operations involved for the following instructions along with respective timing intervals: (i) BSA (ii) ISZ (iii) ADD (b) Explain, why we need to have at least a little portion of primary memory implemented with ROM. 	[2+ (3x4)] +6	CO2, CO4
	OR		
	(c) Discuss about set-associative mapping.(d) Draw the block diagram of CPU registers along with memory in a shared bus architecture. Explain how can the bus be accessed without contention with necessary design mechanism.	[8+(4+ 8)]	