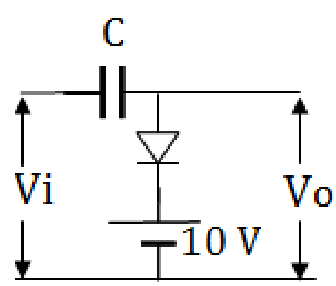
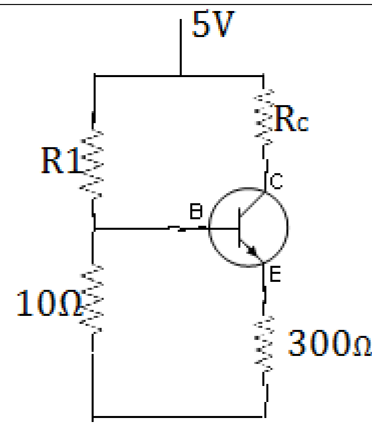
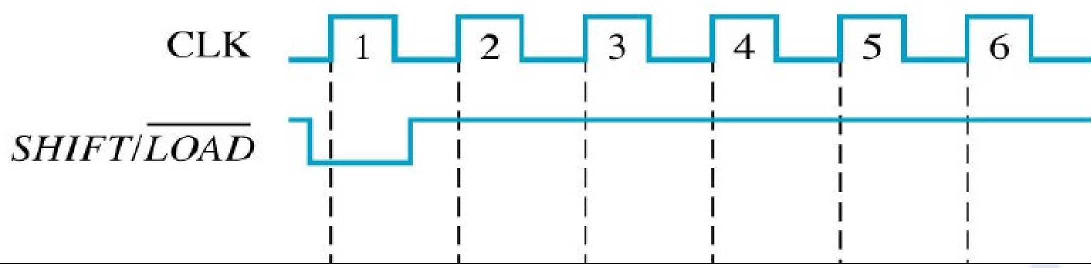
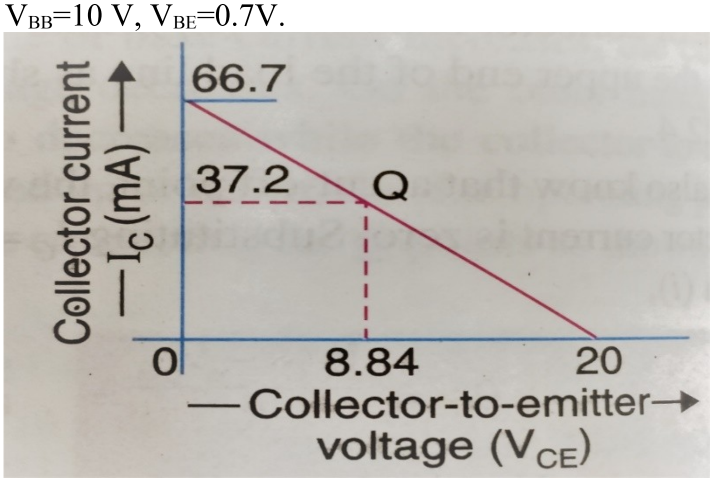
Roll No: --------------------------

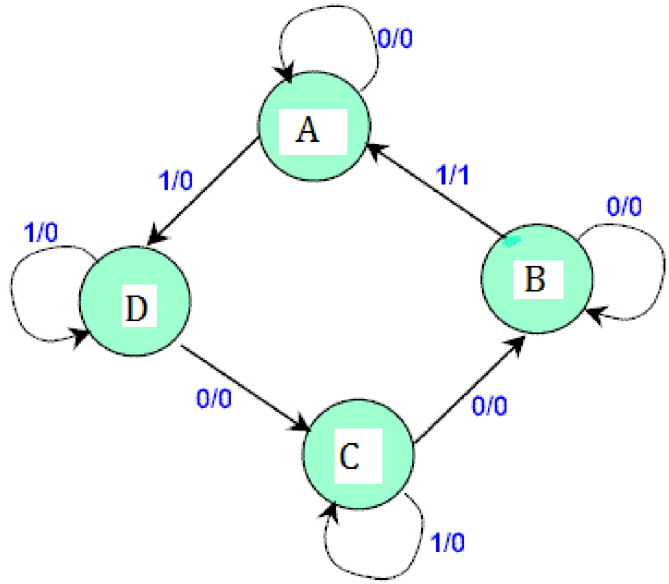
UNIVERSITY OF PETROLEUM AND ENERGY STUDIES

End Semester Examination, December 2017

Program: B.Tech-Electrical Engineering | **Semester – III**
Subject (Course): Analog & Digital Electronics | **Max. Marks : 100**
Course Code :ELEG-216 | **Duration : 3 Hrs**
No. of page/s:03

	SECTION-A	
1.	Draw and explain the circuit diagram of a diode clipper to clip a 5V sine wave input signal at +2V.	**[5]**
2.	Sketch the output wave form of the following figure for a sine wave input with a peak value of 30V. Consider the diode to be Si, Ge and ideal diode cases. 	**[5]**
3.	Minimize the following Boolean function by using K-Map method $F(a,b,c,d) = \sum m(5,6,7,12,13)+\sum d(4,9,14,15)$	**[5]**
4.	Explain the step by step process of implementing a Boolean function by using NAND gates. Implement Ex-NOR gate by using NAND Gate.	**[5]**
	SECTION B	
5.	A Digital system is to be designed in which month of the year is given as the four bit input. January is treated as '0000', February as '0001' and so on. The output of the system should be '1' for the months containing 31 days. Consider the output of other extra inputs as don't care. i. Write the truth table and Boolean expression in SOP form ii. Using K-Map minimize the Boolean function iii. Use 3x8 decoder to implement the output of the system	**[10]**
6.	In the Common Emitter amplifier shown, the transistor has a forward current gain of 100, and a Base to Emitter voltage of 0.6 V. Derive the value for R_1 and R_C such that the transistor has a Collector current of 1 mA and Collector to Emitter voltage of 2.5V.	**[10]**

		
7.	Construct a Parallel In Serial Out shift register for the graph shown below and derive the output graph with the help of the table. Consider the data to be loaded as $D_0D_1D_2D_3$=1010. 	[10]
8.	Design a DC-Power supply with the help of a Bridge rectifier and ∏- Filter. An AC Power supply of 230V is applied to the Bridge rectifier through a transformer of turn's ratio 10:1. Find the DC output voltage, Peak Inverse voltage of the diode, RMS voltage, Efficiency and Ripple factor.	[10]
	SECTION C	
9.	i. Develop a fixed bias circuit for the Load line analysis carried out in the figure. Consider β=200, V_{BB}=10 V, V_{BE}=0.7V.  ii. Implement the following Boolean function by using 2X1 Multiplexer's. $F_1(A, B, C) = \sum m(1,2,4,7)$; $F_2(A, B, C) = \sum m(3,5,6,7)$	[10+10]

10.	Examine the following state graph, Derive the state table and Design the following by using T-FlipFlop's. i. Clocked synchronous sequential circuit. ii. Clocked Asynchronous sequential circuit.  	[20]

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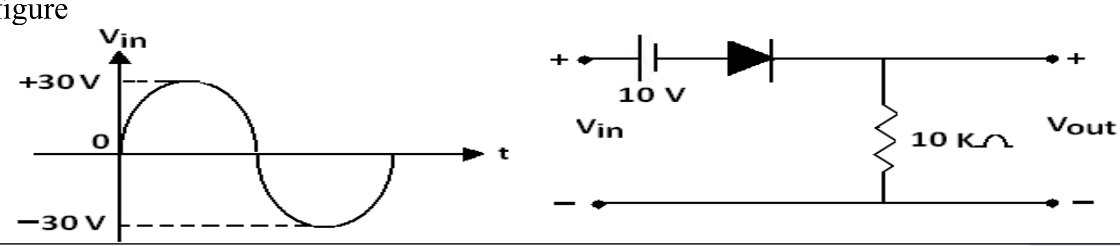
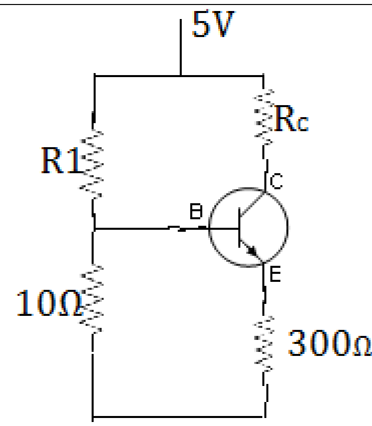
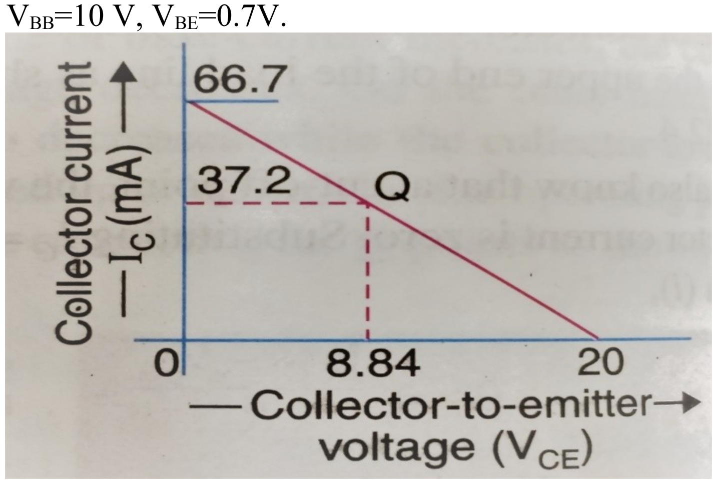
	SECTION-A	
1.	Explain all the types of clippers with neat sketch and sketch the output for the following figure 	**[5]**
2.	Define a clamper circuit, mention the applications. With neat sketch explain the action of **(i) Positive clamper** **(ii) Negative clamper.**	**[5]**
3.	Draw the Internal structure of an 8X1 Multiplexer and write its equation.	**[5]**
4.	What is race around condition and how do we eliminate by using Master-Slave JK FlipFlop.	**[5]**
	SECTION B	
5.	Brief out the timing parameters of the Flipflop's with neat sketch i. Propagation Delay ii. Set-up time iii. Hold time iv. Maximum Clock Frequency	**[10]**
6.	In the Common Emitter amplifier shown, the transistor has a forward current gain of 100, and a Base to Emitter voltage of 0.6 V. Derive the value for R_1 and R_C such that the transistor has a Collector current of 1 mA and Collector to Emitter voltage of 2.5V.	**[10]**

		
7.	Implement a Full adder by using 2x4 decoder's.	**[10]**
8.	A 50Ω load resistor is connected across a full wave rectifier. The peak amplitude (V_m) is given as 103.5V. Calculate the DC-output voltage, RMS voltage, Ripple factor, Peak inverse Voltage and Efficiency of the rectifier.	**[10]**
	SECTION C	
9.	i. Develop a fixed bias circuit for the Load line analysis carried out in the figure. Consider β=200, V_{BB}=10 V, V_{BE}=0.7V.  ii. A Digital system is to be designed in which month of the year is given as the four bit input. January is treated as '0000', February as '0001' and so on. The output of the system should be '1' for the months containing 31 days. Consider the output of other extra inputs as don't care. i. Write the truth table and Boolean expression in SOP form ii. Using K-Map minimize the Boolean function iii. Use logic gates to implement the output of the system	**[10+10]**
10.	i. Design an BCD- Excess3 code converter. ii. Implement an JK-Flipflop by using T-Fliflop's iii. Design a synchronous counter which counts in the sequence of 0→4→5→2→1→6→7→3 by using D-Flip flops.	**[6+6+8]**