Name:

Enrolment No:

UNIVERSITY OF PETROLEUM AND ENERGY STUDIES
End Semester Examination, December 2018

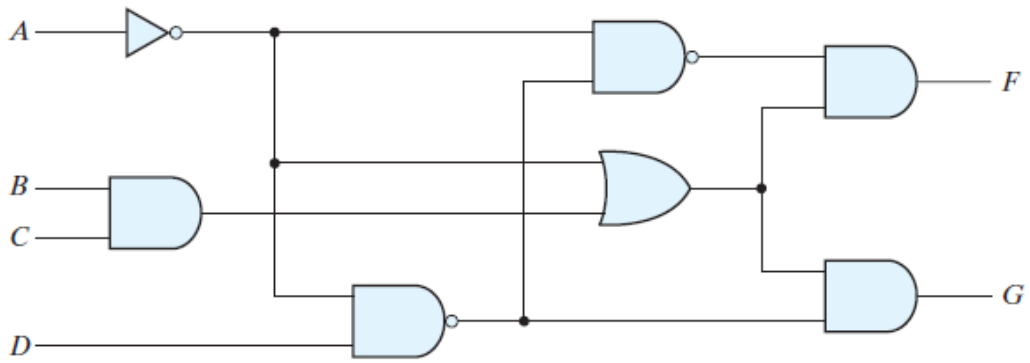
Course: Digital Electronics **Semester: III**
Programme:B.Tech ASE-A
Time: 03 hrs. **Max. Marks: 100**
Instructions:

SECTION A
All questions are compulsory

S. No.		Marks	CO
Q1	Draw the logic diagram of a SR latch using NOR gates. Explain its Operation using Excitation table.	**4M**	**CO3**
Q2	Discuss the difference between combinational logic and sequential logic circuits	**4M**	**CO3**
Q3	(a)Convert the decimal number 430 to Excess-3 code (b) Convert the gray code 1011001100 into its binary	**(2+2)**	**CO1**
Q4	Implement the following function using suitable multiplexer F= Σm(0,2,5,7)	**4M**	**CO2**
Q 5	What are universal gates. Construct a logic circuit using NAND gates only for the Expression x = A . (B + C).	**4M**	**CO1**

SECTION B
All questions are compulsory and each carries 10 marks. Internal choice for Qno 9

Q 6	Design a 4-bit universal shift register and draw the circuit with the given mode of operation table 1 S1 | S0 | Operation 0 | 0 | Parallel 0 | 1 | Shift right 1 | 0 | Shift left 1 | 1 | Inhibit clock Table 1	**10M**	**CO4**
Q 7	(A) Prove the following Boolean identities using the laws of Boolean algebra: (i) $(A + B)(A + C) = A + BC$ (ii) $ABC + ABC + ABC = A(B + C)$ (B) Obtain the simplified expression for the output F and G in terms of the input	**[4+6]**	**CO1+ C02**

	variables for the circuit shown in figure 1  Figure 1		
Q 8	Describe the working of Master Slave J-K flip flop and explain the Race Around condition	**10M**	**CO5**
Q 9	(a)Implement a 2 bit magnitude comparator using a suitable decoder (or) (b) Show that the characteristic equation for the output of a SR flip flop is Q(n+1)=S+R'Qn	**10M**	**CO1+ CO2**
SECTION-C **All questions are compulsory and each carries 20 marks. Internal choice for Qno 11**			
Q 10	(a)Design a 4-bit Asynchronous up/down counter (b) Show how an SR flip flop can be converted into a JK flip flop	**20M**	**CO5**
Q 11	(a) Design a 3-bit binary-to gray code converter using suitable PLA (b) Design the circuit diagram of common cathode BCD to seven-segment display (or) (C) Solve the following using Quine Mc- Clusky method $F(x_1, x_2, x_3, x_4, x_5) = \sum(0,1,4,5,6,7,8,10,14,17,18,21,29,31)$.	**20M**	**CO4+ CO3**

Name: **Enrolment No:**	UPES

UNIVERSITY OF PETROLEUM AND ENERGY STUDIES
End Semester Examination, December 2018

Course: Digital Electronics **Semester: III**
Programme:B.Tech ASE-A
Time: 03 hrs. **Max. Marks: 100**
Instructions:

SECTION A
All questions are compulsory

S. No.		Marks	CO
Q1	What do you mean by "MUX"? Implement the 4:16 MUX and what will be the output of mux if we connect the select lines with logic"1101″?	**4M**	**CO3**
Q2	Draw the logic diagram of a D flip flop . Explain its Operation using Excitation table	**4M**	**CO2**
Q3	Encode the following decimal number in BCD code: 1. 327.89 2. 46	**4M**	**CO1**
Q4	Write the short notes on following (a) PIPO (b) SISO	**4M**	**CO2**
Q 5	Apply demorgan's theorem and simplify ((A+BC')'+D(E+F')')'	**4M**	**CO1**

SECTION B
All questions are compulsory and each carries 10 marks. Internal choice for Qno 9

Q 6	Design a neat circuit diagram of a 4-bit bidirectional shift register using D- flip flop having right and left data inputs and mode control M such that M=0 left shift, M=1 right shift	**10M**	**CO5**
Q 7	A combinational logic circuit has 4 inputs and two outputs F1 and F2.The output F1 gives high output when the input combinational is greater than or equal to 1001,otherwise low output. The output F2 gives high output when the input combination is less than 1001 otherwise the output F2 is LOW Implement it by using PLA.	**[10M]**	**CO2**
Q 8	Implement the Full subtractor combinational logic circuit using multiplexer.	**10M**	**CO3**
Q 9	(a) Design a 4-bit down/up ripple Asynchronous counter (or) (b) Design and explain the block diagram of an 4-bit parallel adder/substractor and explain its limitations.	**10M**	**CO3+ CO2**

SECTION-C **All questions are compulsory and each carries 20 marks. Internal choice for Qno 11**			
Q 10	(a) Design the realization of SR flip-flop, JK flip-flop using D flip-flop. (b) Design a 3-bit gray-to binary code converter using suitable PLA	**20M**	**CO5**
Q 11	(a) Design and explain a synchronous MOD-12 down-counter using J-k flip-flop (b) Design and explain a 4-bit ring counter using D-flip flops with relevant timing diagrams. (or) C) Solve the following using Quine Mc- Clusky method $F(x_1, x_2, x_3, x_4, x_5) = \sum(0,1,4,5,6,7,8,10,14,17,18,21,29,31) + \sum d(11,20,22)$	**20M**	**CO4+ CO1**