Name: Enrolment No:	UPES

UNIVERSITY OF PETROLEUM AND ENERGY STUDIES

End Semester Examination, December 2018

Programme Name: B Tech EE, EE-BCT **Semester : V**
Course Name : Linear Integrated Circuits **Time : 03 hrs**
Course Code : ELEG263 **Max. Marks : 100**
Nos. of page(s) : 4
Instructions:

- Attempt all questions as per the requirement.
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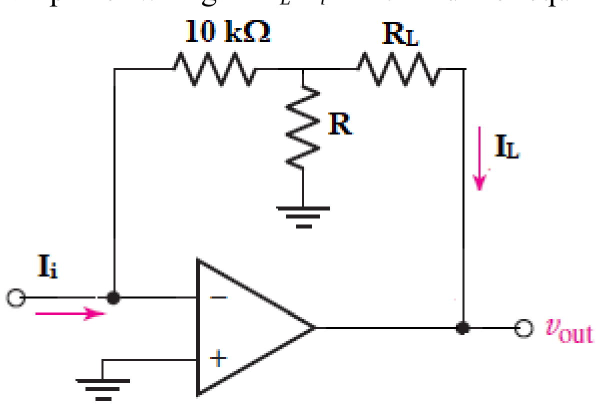
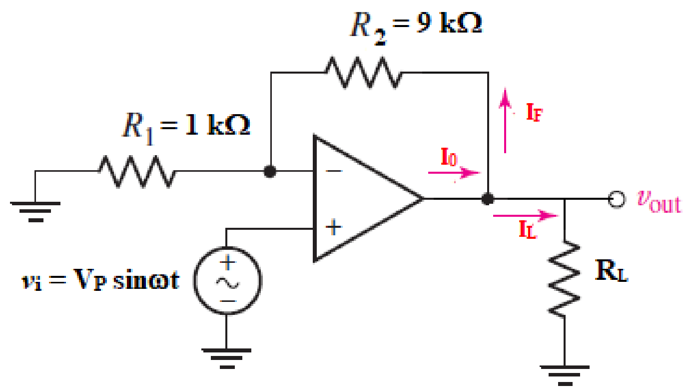
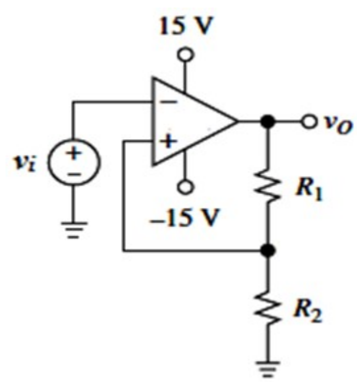
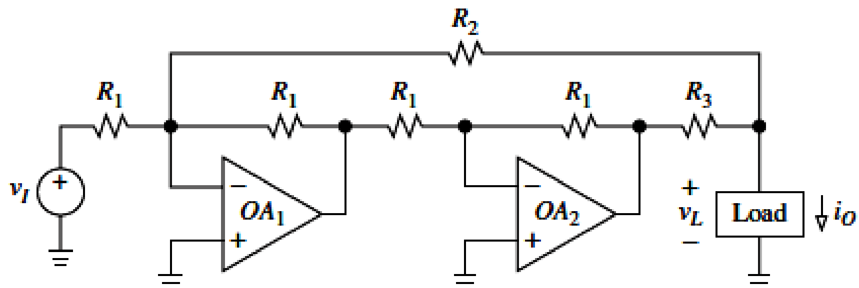
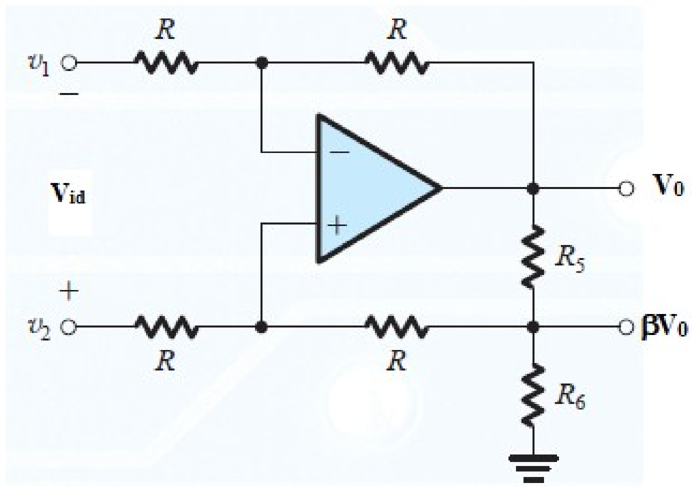
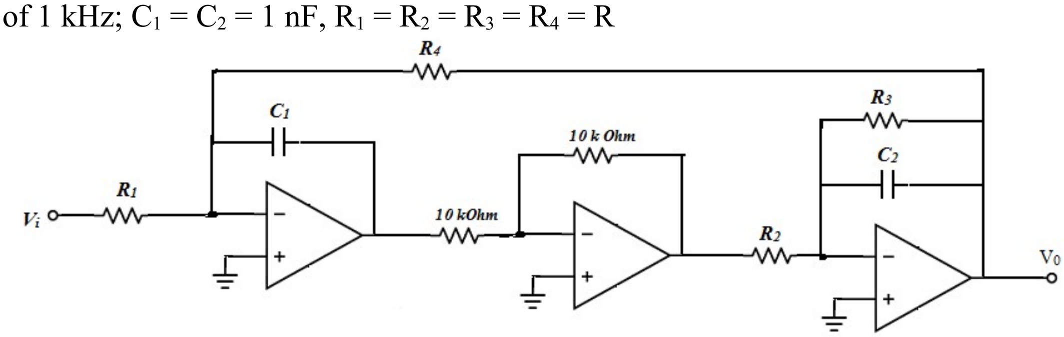
- Strike off all unused blank pages

SECTION A (20 Marks)

S.No.		Marks	CO
Q1	Describe briefly the block diagram of op-amp.	4	CO1
Q2	Assuming the op amp to be ideal, it is required to design the circuit shown in **Fig.1** to implement a current amplifier with gain $I_L/I_i=10$. Find the required value for R.  **Fig. 1**	4	CO2
Q3	What is meant by filter? Give comparison between passive and active filters.	4	CO3
Q4	Write the important features of 555 timer. And also draw the pin diagram of 8-pin DIP 555 timer.	4	CO4
Q5	An 8-bit ADC is capable of accepting an input voltage 0 to 10 V. (a) what is the minimum value of input voltage to cause a digital output change of 1 LSB? (b) What is the digital output code if the applied input voltage is 5.2 V?	4	CO5

SECTION B (40 Marks)			
Q6	Consider the noninverting amplifier circuit shown in **Fig.2**. As shown, the circuit is designed for a nominal gain $1+\frac{R_2}{R_1}$ It is fed with a low-frequency sine-wave signal of peak voltage V_p and is connected to a load resistor R_L. The op amp is specified to have output saturation voltages of ±13 V and output current limits of ±20 mA. **(a)** For V_p = 1V and R_L = 1 kΩ, calculate v_0, i_L, i_F, i_0 for the signal resulting at the output of the amplifier. **(b)** For R_L = 1 kΩ, what is the maximum value of Vp for which an undistorted sine-wave output is obtained? **(c)** For V_p = 1 V, what is the lowest value of R_L for which an undistorted sine-wave output is obtained?  **Fig. 2**	**8**	**CO1**
Q7	A regenerative comparator (Schmitt Trigger) circuit is shown in **Fig. 3** (i) Derive expressions for upper threshold and lower threshold voltages, V_{UT} and V_{LT} respectively and hence the value of hysteresis voltage V_H. Calculate V_{UT}, V_{LT}, V_H for the given values of R_1 = 27 kΩ and R_2 = 1 kΩ. (ii) A sine wave with 2 V peak-to-peak amplitude and 1 kHz frequency is app lied at the input of the circuit. Plot the input and output waveforms. Vcc = + 15 V  **Fig. 3** **OR** Draw the generalized circuit diagram of Sallen key second order filter and derive the transfer function of it.	**8**	**CO3**

Q8	Draw the block diagrams of the 555 timer Show how 555 can be used as mono-stable multi-vibrator. Describe the circuit operation with the help of waveforms and derive an expression for the frequency of oscillations	**8**	**CO4**
Q9	Explain the following op-amp circuits: V-I converter; integrator and differentiator; logarithmic amplifier **Or** Given that the circuit of **Fig.4** yields $i_0 = AV_i - \frac{V_L}{R_0}$, find the expressions for A and R_0  **Fig. 4**	**8**	**CO2**
Q10	What are the advantages of R-2R ladder type DAC over weighted binary resistor type? Explain a 4-bit R-2R ladder type DAC in detail.	**8**	**CO5**
	SECTION-C (40 Marks)		
Q11	**(a)** To obtain a high-gain, high-input-resistance difference amplifier, the circuit in **Fig.5** employs positive feedback, in addition to the negative feedback provided by the resistor *R* connected from the output to the negative input of the op amp. Specifically, a voltage divider (R_5, R_6) connected across the output feeds a fraction β of the output, that is, a voltage β V_0, back to the positive-input terminal of the op amp through a resistor *R*. Assume that R_5 and R_6 are much smaller than *R* so that the current through *R* is much lower than the current in the voltage divider, with results that $\beta \cong \frac{R_6}{R_5+R_6}$. Show that the differential gain is given by $A_d = \frac{V_0}{V_{id}} = \frac{1}{1-\beta}$	**10+10**	**CO2**

	 **Fig. 5** Design the circuit to obtain a differential gain of 10. Select values for R, R_5, and R_6, such that $R_5 + R_6 \leq R/100$ **(b)** Design an inverting op-amp circuit to form the weighted sum V_0 of two inputs V_1 and V_2. It is required that $V_0 = -(V_1 + 5\ V_2)$. Choose values for R_1, R_2, and R_F so that for a maximum output voltage of 10 V the current in the feedback resistor will not exceed 1 mA.		
Q12	**(a)** Design an astable multi-vibrator using 555 timer for an oscillating frequency of 10 kHz and a duty cycle of 70%. Assume C = 0.1 μF **(b)** Design a Multi-feedback second order band pass filter (assume the standard circuit) with bandwidth 10% of center frequency. Given that the center frequency is 10 kHz and R = 1 kΩ **OR** The circuit diagram shown in the **Fig.6** is the second order active low pass filter. Determine the transfer function and hence determine the cut-off frequency. Design this filter with the following parameters: Gain = 20 dB and cut off frequency of 1 kHz; $C_1 = C_2 = 1$ nF, $R_1 = R_2 = R_3 = R_4 = R$  **Fig.6**	**20**	**CO4**

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SECTION A (20 Marks)

S.No.		Marks	CO
Q1	Distinguish between input bias current and input off-set current in op-amp. And then calculate the input bias and off-set currents for an op-amp with input currents 8.3 μA and 7.9 μA.	4	CO1
Q2	Derive the expression of gain for inverting and non-inverting op-amp amplifier.	4	CO2
Q3	Explain the operation of the switched capacitor circuit with necessary circuit diagram and equations	4	CO3
Q4	Define three states in Phased Locked Loop (PLL): free running; capture; phase lock	4	CO4
Q5	A six-bit A/D converter has a maximum precision supply voltage of 20 V. What voltage change does each LSB represent? What voltage does 100110 represent?	4	CO5

SECTION B (40 Marks)

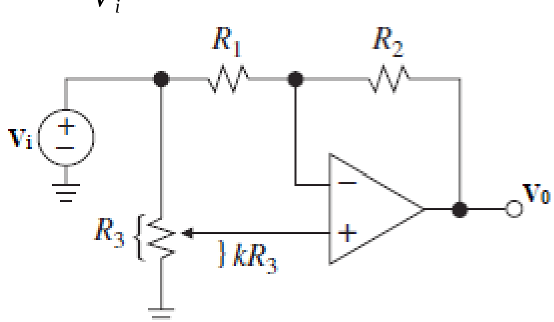
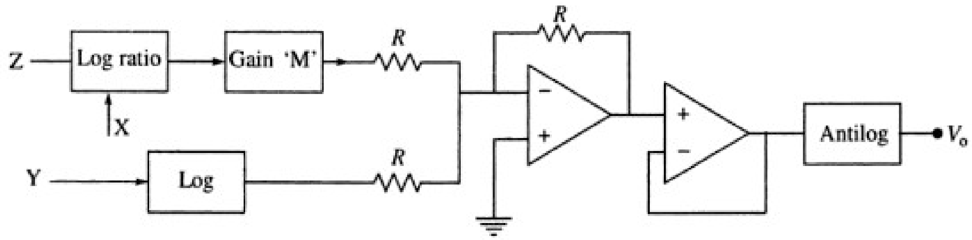
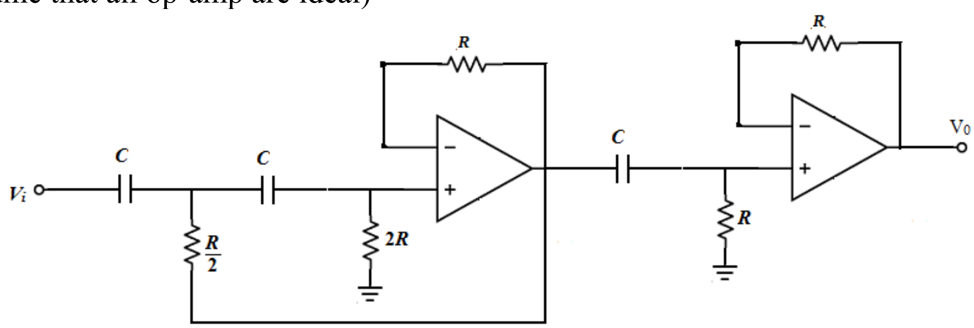
Q6	In the circuit of **Fig. 1** the pot is used to control gain magnitude as well as polarity. Letting k denote the fraction of R_3 between the wiper and ground, show that varying the wiper from bottom to top varies the gain over the range $-R_2/R_1 \le \frac{V_0}{V_i} \le 1$, so that making $R_1 = R_2$ yields $-1 \le \frac{V_0}{V_i} \le +1$. 	8	CO1

	Fig. 1		
Q7	(a) Explain the following op-amp circuit: sample and hold circuit (b) Determine the output of the circuit shown in **Fig.2**  **Fig.2**	**5+3**	**CO2**
Q8	**(a)** Sketch and explain operation of the circuit of a 555 timer connected as an astable multi-vibrator. **(b)** If the frequency of the oscillations of astable multi-vibrator using 555 timer is 350 kHz, determine the value of capacitor C needed using $R_A = R_B = 7.5$ kΩ	**6+2**	**CO4**
Q9	Determine the transfer function of 3rd order filter as shown in **Fig. 3** and then determine the type of filter (LP, HP, BP or BS filter) and its cut-off frequency. (assume that all op-amp are ideal)  **Fig. 3** **(Or)** Explain the operation of pulse wave form generator using op-amp. Also derive the expression for pulse width of the output signal.	**8**	**CO3**
Q10	Describe the operation of dual slope ADC with necessary diagrams. **Or** **Fig. 4** shows a circuit for a digital-to-analog converter (DAC). The circuit accepts a 4-bit input binary word $a_3a_2a_1a_0$, where a_0, a_1, a_2, and a_3 take the values of 0 or 1, and it provides an analog output voltage V_0 proportional to the value of the digital input. Each of the bits of the input word controls the correspondingly numbered switch. For instance, if a_2 is 0 then switch S_2 connects the 20 kΩ resistor to ground, while if a_2 is 1 then S_2 connects the 20 kΩ resistor to the +5 V power supply. Show that V_0 is given by	**8**	**CO5**

$$V_0 = -\frac{R_f}{10}\frac{V_R}{2^n}\left(2^3 a_3 + 2^2 a_2 + 2^1 a_1 + 2^0 a_0\right)$$

Where R_f is in kΩ. Find the value of R_f so that V_0 ranges from 0 to -12 volts.

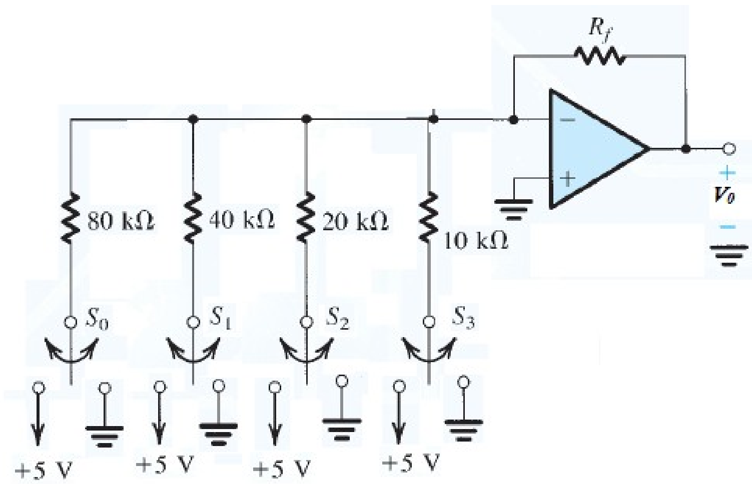


Fig. 4

SECTION-C (40 Marks)

Q11

(a) Design a Saalen key 2nd order high pass filter shown in **Fig.5** with a cut-off frequency of 1 kHz, a voltage gain of 20 dB and a quality factor (Q) of 5. Given that $R_1 = R_2 = 1$ kΩ

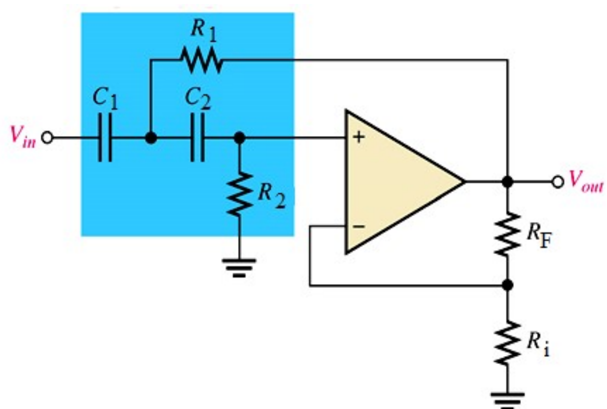


Fig. 5

(b) A PLL IC565 connected as an FM detector has R_T = 10 kΩ, C_T = 0.01µF and C = 0.04 µF. the supply voltage is +12 V. Determine the free running frequency, lock range and capture range.

(c) Assume you have a 4-bit Successive Approximation type ADC. For the analog input 0.25V; 1.5 and 1.75 V, show how the SAR would approximate the analog input with relevant diagrams. (Given that the V_{ref} is 4V)

10+5+5

CO3 +CO4 +CO5

Or

<table>
<tr>
<td></td>
<td>The filter circuit of Fig.6 provides the low-pass and band-pass responses using only two op amps. (i) Show that $A_{0BP} = V_{BP}/V_i = -n$, $A_{0LP} = V_{LP}/V_i = m/(m+1)$, $Q=\sqrt{n(1+1/m)}$, and $\omega_0=Q/nRC$. (ii) Specify component values for a band-pass response with $f_0 = 2$ kHz and $Q = 10$. (iii) What is the resonance gain of your circuit?

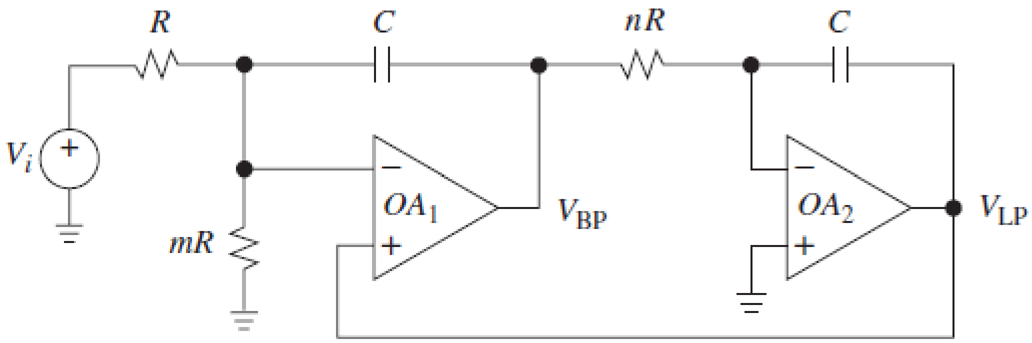


Fig. 6</td>
<td>20</td>
<td>CO3</td>
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<tr>
<td>Q8</td>
<td>(a) Design a circuit depicted in Fig. 7, whose output is $V_O = V_{i1} + 3V_{i2} - 2(V_{i3} + 3V_{i4})$.

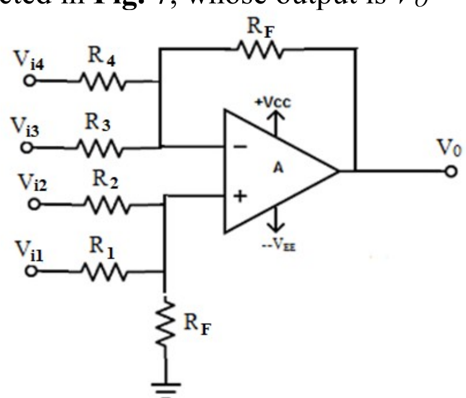

Fig. 7
(b) Design an op-amp circuit to solve the following differential equation
$$A\frac{d^2V_0}{d^2t}+B\frac{dV_0}{dt}+CV_0=V_i$$
Where A, B and C are constants. V_0 and V_i are the time dependent voltages.</td>
<td>10+10</td>
<td>CO2</td>
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