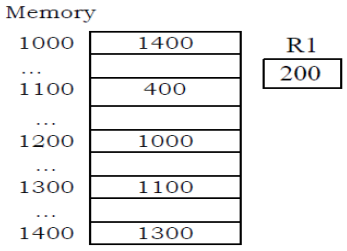
Name:	UPES
Enrolment No:	

UNIVERSITY OF PETROLEUM AND ENERGY STUDIES

End Semester Examination, November/ December 2018

Program Name: B.Tech (CSE-All Courses)
Semester : III
Course Name : Computer System Architecture **Time : 03 hrs**
Course Code : CSEG2004 **Max. Marks : 100**
Nos. of page(s) : 03
Instructions: Answer the following questions

SECTION A

S. No.		Marks	CO
Q1	Design a 4 to 2 bit Priority Encoder?	5	CO2
Q2	Solve using K Map: i) $F(A, B,C,D) = \pi M(0,3,4,7,8,10,12,14)+ d(2,6)$ ii) $F(W,X,Y,Z) = \sum m(0,7,8,9,10,12) + d(2,5,13)$	(2.5 X 2=5)	CO2
Q3	Answer the following: i) What is the advantage of having input output processors in the computer system when we have processor/CPU which can also do input output transfers? ii) Give two differences between memory-mapped I/O and isolated I/O. iii) Convert binary number $(1\ 1\ 1\ 1\ 1\ 0\ 1\ 1.\ 1\ 0\ 0\ 1\ 0\ 1)_2$ to decimal, hexadecimal and Octal number. iv) Differentiate between Combinational and Sequential Circuits	(1+1+2+1 =5)	CO5, CO2
Q4	Suppose we have the instruction Load 1000. Given memory and register R1 contain the values below:  Assuming register R2 has content as 1300, determine the actual value loaded into the accumulator. Show the appropriate calculation wherever needed: i) Immediate ii) Direct iii) Indirect	(5)	CO1

	iv) Indexed with R1 as Index register v) Register indirect taking R2 in consideration		
	SECTION B		
Q5	The content of PC in the basic computer is 3AF (all numbers in hexadecimal). The content of AC is 7EC3. The content of memory at address 3AF is 932E. The content of memory at address 32E is 09AC.The content of memory at address 9AC is 8B9F. Assume the opcode for binary pattern 001 is ADD i) What is the instruction that is fetched and executed first? ii) Show the binary operation that will be performed in the AC when the instruction is executed. iii) Give the contents of registers PC, AR, DR, AC and IR in hexadecimal and the values of E, I and the sequence counter SC in binary at the end of the instruction cycle. iv) Leaving the above scenario, starting from an initial value of R = 11011101, determine the sequence of binary values in Register R after a logical shift-left, followed by a circular shift-right, followed by a logical shift-right and a circular shift-left.	**(2.5 x 4=10)**	**CO3**
Q6	**A.** Match the column A to the best option from column B. Column A: 1.Multicomputer; 2.ROM; 3.Main memory; 4. Cache memory; 5.Hardware interlock Column B: 1.Dynamic memory; 2.Locality of reference; 3.Firmware; 4.Data dependency; 5.Clusters **B.** There are 128 x 8 RAM chips. i) How many 128 x 8 RAM chips are needed to provide a memory capacity of 2048 bytes? ii) How many lines of the address bus must be used to access 2048 bytes of memory? iii) How many of these lines will be common to all chips? iv) How many lines must be decoded for chip select? Specify the size of the decoder. v) Show with the diagram, how the chips are to be actually connected to the address lines .Also show the memory address mappings for each row of the RAM chips.	**(5)** **(1 X 5 =5)**	**CO5**
Q7	What do you understand by Priority Interrupt? Explain with the help of suitable diagram, the Sequential Hardware method of solving the Priority Interrupt?	**(2+8=10)**	**CO5**
Q8	Explain in detail the Instruction Cycle? Differentiate between Branch Unconditionally (BUN) and Branch and Save Return Address (BSA) memory reference Instructions **OR** What are the different types of Interrupts? Explain the Interrupt Cycle with the help of	**(5+5=10)**	**CO3**

	suitable diagram		
	SECTION-C		
Q9	**A.** An instruction pipeline has five stages where each stage take 2 nanoseconds and all instruction use all five stages. Branch instructions are not overlapped. i.e., the instruction after the branch is not fetched till the branch instruction is completed. Under ideal conditions, i) Calculate the average instruction execution time assuming that 20% of all instructions executed are branch instruction. Ignore the fact that some branch instructions may be conditional. ii) If a branch instruction is a conditional branch instruction, the branch need not be taken. If the branch is not taken, the following instructions can be overlapped. When 80% of all branch instructions are conditional branch instructions, and 50% of the conditional branch instructions are such that the branch is taken, calculate the average instruction execution time. **B.** Consider a 5-stage pipeline - IF (Instruction Fetch), ID (Instruction Decode and register read), EX (Execute), MEM (memory), and WB (Write Back). All (memory or register) reads take place in the second phase of a clock cycle and all writes occur in the first phase. Consider the execution of the following instruction sequence: I1: sub r2, r3, r4; /* r2←r3−r4 */ I2: sub r4, r2, r3; /* r4←r2−r3 */ I3: sw r2, 100(r1) /* M[r1+100]←r2 */ I4: sub r3, r4, r2 /* r3←r4−r2 */ i) Show all data dependencies between the four instructions. ii) Identify the data hazards. iii) Can all hazards be avoided by forwarding in this case?	**(5+5=10)** **(3+4+3=10)**	**CO3**
Q10.	Explain the complete procedure of address Sequencing (address calculation) of microinstructions present in control memory in a microprogrammed control unit with the help of suitable diagram. **OR** Assume there is a control memory having 1024 words of 32 bits each. The format of control word is as shown: Condition select | Branch address Field | Microoperation Field The Microperation field has 16 bits. i) How many total bits are there in the control address register? ii) How many bits are there in the branch address field and the condition select field? iii) If there are 16 status bits in the system, how many bits of the branch logic are used to select a status bits? iv) How many bits are left to select an input for the multiplexers? v) Using mapping procedure, find the first microinstruction address of 7 bits from the following 4 bits operation code: a) 1010 b)1100 vi) Explain the difference between Hardwired and Microprogrammed Control. Is it possible to have a hardwired control associated control	**(20)** **(2+2+2+2+2+10=20)**	**CO4**

	associated with a control memory?		

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Course Code : CSEG2004 **Max. Marks : 100**
Nos. of page(s) : 04
Instructions: Answer the following questions

SECTION A

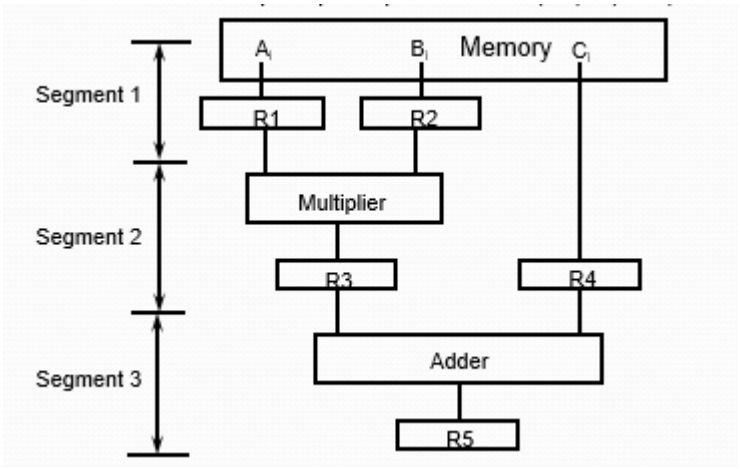
S. No.		Marks	CO
Q1	Convert SR to T Flip Flop	**5**	**CO2**
Q2	Solve using K Map: i) $F(A, B,C,D) = \pi M(0,2,3,8,9,12,13,15)$ ii) F(A,B,C,D)=A' (bar) B' (bar) D+ABC' (bar) D' (bar)+A' (bar)BD+ABCD' (bar) **Note**: ' symbol here denoted negation(bar)	**(2.5 X 2)**	**CO2**
Q3	Answer the following: i) What is the advantage of handshaking asynchronous data transfer technique over strobe control? ii) Give two differences between RISC and CISC architecture. iii) Convert binary number $(1\ 1\ 1\ 1\ 1\ 1\ 1\ 1.\ 1\ 0\ 0\ 1\ 0\ 1)_2$ to decimal, hexadecimal and Octal number. iv) The 8 bit Registers AR,BR, CR and DR initially have the following values: AR=11110010 BR=11111111 CR=10111001 DR=11101010 Determine the 8 bit values in each register after the execution of the following sequence of micro operations. AR ←AR+ BR Add BR to AR CR ← CR ∧ DR, BR ← BR+1 AND DR to CR, increment BR	**(1+2+2+1)**	**CO5, CO2**
Q4	An instruction is stored at location 300 with its address fields at location 301. The address field has the value 400. A processor register RI contain the number 200. Evaluate the effective address if the addressing mode of the instruction is	**(1x 5)**	**CO1**

	i) Direct ii) Immediate iii) Relative iv) Register Indirect v) Index with RI as the Index register.		
	SECTION B		
Q5	A Computer uses a memory of 65,536 words with eight bits in each word. It has the following registers: PC, AR, TR (16 bits each) and AC, DR, IR (8 bits each). A memory Reference Instruction consists of three words: an 8 bit OP code (one word) and a 16 bit address (in next two words). All operands are 8 bits. There is no indirect bit. i) Draw a block diagram of the computer showing the memory and registers. (Don't use common bus) ii) Draw a diagram showing the placement in memory of a typical three word instruction and the corresponding 8 bit operand. iii) List the sequence of micro Operations for fetching a memory reference instruction and then placing the Operand in DR. Start from timing signal T_0	**(3+3+4)**	**CO3**
Q6	a) Match the column A to the best option from column B. Column A: 1.BootStrap Loader; 2. Associative Mapping; 3. Associative memory; 4. Logical Address; 5. Auxiliary Memory Column B: 1. Magnetic Disks; 2. Content Addressable Memory; 3. Cache Memory; 4. ROM; 5. CPU b) A digital computer has a memory unit of 64K x 16 and a cache memory of 1K words. The cache uses direct mapping with a block size of four words. i) How many bits are there in the tag, index, block and word fields of the address format? ii) How many bits are there in each word of cache, and how are they divided into functions? Include a valid bit. iii) How many blocks can the cache accommodate?	**(5)** **(2+2+1)**	**CO5**
Q7	What are the different types of Interrupts? Explain the Interrupt Cycle with the help of suitable diagram.	**(3+7)**	**CO3**
Q8	What do you understand by Priority Interrupt? Explain with the help of suitable diagram, Daisy Chaining Sequential Hardware solution of solving the Priority Interrupt? OR Explain in detail the process of DMA transfer. State clearly the meaning of cycle stealing.	**(3+7)** **(6+4)**	**CO5**

SECTION-C

Q9

A.



$R_1 \leftarrow A_i$, $R_2 \leftarrow B_i$
$R_3 \leftarrow R_1 * R_2$, $R_4 \leftarrow Ci$
$R_5 \leftarrow R_3 + R_4$

The pipeline for the above operations has the following propagation times; 40 ns for the operands to be read from memory into registers R1 and R2, 45 ns for the signal to propagate through the multiplier, 5 ns for the transfer into R3 and 15 ns to add the two numbers into R5.

i) What is the minimum clock cycle time that can be used?
ii) A non-pipeline system can perform the same operation by removing R3 and R4. How long will it take to multiply and add the operands without using pipeline?
iii) Calculate the speedup of the pipeline for 10 tasks and again for 100 tasks.
iv) What is the maximum speed up that can be achieved.

(2+3+3+2)

B. Consider a 5-stage pipeline - IF (Instruction Fetch), ID (Instruction Decode and register read), EX (Execute), MEM (memory), and WB (Write Back). All (memory or register) reads take place in the second phase of a clock cycle and all writes occur in the first phase. Consider the execution of the following instruction sequence:

```
I1:   sub r2, r3, r4;  /*      r2←r3−r4      */
I2:   sub r4, r2, r3;  /*      r4←r2−r3      */
I3:   sw r2, 100(r1) /*      M[r1+100]←r2        */
I4:   sub r3, r4, r2   /*      r3←r4−r2      */
```

i) Show all data dependencies between the four instructions.
ii) Identify the data hazards.
iii) Can all hazards be avoided by forwarding in this case?

(3+4+3)

CO3

Q10	Explain the complete procedure of address Sequencing (address calculation) of microinstructions present in control memory in a microprogrammed control unit with the help of suitable diagram. **OR** Differentiate between a microprocessor and a microprogram? Is it possible to design a microprocessor without a microprogram? Are all microprogrammed computers also microprocessors? The control memory has 4096 words of 24 bits each. i) How many bits are there in the Control Address Register? ii) How many bits are there in each of the four inputs, going into the multiplexers? iii) What are the number of inputs in each multiplexer and how many multiplexers are needed?	**(20)** **(10+4+2+2+2)**	**CO4**