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UPES

UNIVERSITY OF PETROLEUM AND ENERGY STUDIES

End Semester Examination, May 2018

Program: B.Tech (EE+IoT) **Semester – IV**
Subject (Course): Digital Electronics **Max. Marks : 100**
Course Code : ELEG220 **Duration : 3 Hrs**
No. of page/s: 02

SECTION A

Note: All questions are compulsory & carry equal marks. (5x4=20)

Q1. Design a two bit Binary to Gray code converter CO1
Q2. Convert the SOP form into POS for the expression- AB'+BC+ABC CO2
Q3. Minimize the function with K-Map- F(A,B,C,D)= ΠM(0,2,4,5,6,7,9,12).d(3,14) CO2
Q4. Design full adder with 4:1 MUX gates. CO1

SECTION B

Note: All questions are compulsory & carry equal marks. (10x4=40)

Q5. (i) Discuss a four bit Parallel IN Serial OUT right shift register with the help of circuit diagram and example CO4
Q6. (i) Draw the state diagram, truth table, excitation table and characteristics equation for T Flip Flop
(ii) Convert J-K flip flop into D Flip Flop. Also discuss the race around condition. CO4

Q7. Reduce the function with Q-M method and verify it with K-Map-
F(A,B,C,D)= ∑(5,7,13,15)+d(4,6,12,14) CO2
Q8. Design and discuss four bit BCD adder. Differentiate it from parallel adder CO3

SECTION C

Note: All questions carry equal marks. Q10 has internal choice and Q9 is compulsory

(20x2=40)

Q.9 (i) Design a common anode BCD to seven segment converter, with the help of Truth table, K-Map and logic gates. CO3

(ii) Design a Asynchronous Mod-12 Counter with 'T' Flip Flop CO3

Q.10 Design a synchronous sequence generator with the help of J-K flip flop, which can generate a sequence of 11001011. Draw the state diagram, truth table, circuit diagram and waveform.

Or

Design a three bit UP?DOWN counter with J-K flip flop. Draw the state diagram, truth table, circuit diagram and waveform. CO4