Name: Enrolment No:	UPES

UNIVERSITY OF PETROLEUM AND ENERGY STUDIES
End Semester Examination, April/May 2018

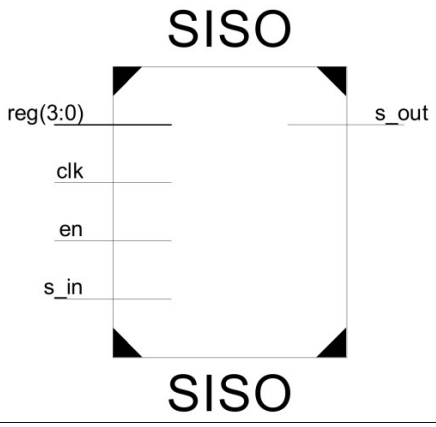
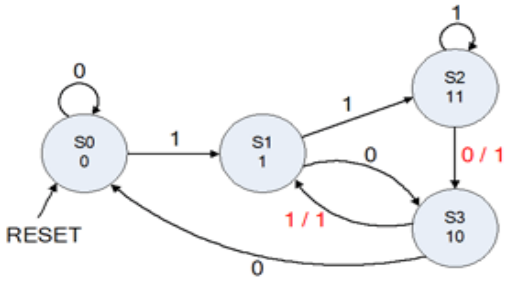
Course: VHDL **Code: ELEG-434**
Semester: VIII **Program: B. Tech/EE**
Time: 03 hrs. **Max. Marks: 100**

SECTION A

S. No.		Marks	CO
Q 1	Write concurrent code for 8 to 1 Mux using WHEN-ELSE statement	**5**	**CO3**
Q2	Explain the Behavioral domain, Structural domain and Physical domain of system to silicon level VLSI Design.	**5**	**CO2**
Q3	List out the salient features MAX 7000 series CPLD with neat sketch. And also explain about the structure of CLB's and Slices in the FPGA architecture.	**5**	**CO1**
Q4	Derive the circuit for the piece of Verilog code given below and write the code at dataflow level. **module electronics(x,clock,Q1,Q2)** **input x, clock;** **output reg Q1, Q2;** **always@(posedge clock)** **begin** **Q1=x;** **Q2= Q1;** **end** **end module**	**5**	**CO4**

SECTION B

Q5	Mention all the types of pre-defined data types, operators and data & signal attributes in VHDL. And also Mention the output for the following. i. W <= (0 =>'1', OTHERS => '0'); ii. d'Reverse_range of **Signal d:std_logic_vector(7 downto 0);** iii. If x<="1001010" then Y<= x sra 4	**10**	**CO1**
Q6	Write the VHDL code for the following RTL diagram of the SISO shift register. Consider the data"1010" given to SISO shift register, with neat sketch the output graph after simulation and also explain the step by step procedure of data transfer w.r.t clock pulse.	**10**	**CO3**

			
Q7	Write 4 bit Parallel adder structural VHDL code using fulladder as component	**10**	**CO3**
Q8	Analyze the following design terms in the VLSI design cycle a) Architectural Design b) Functional Design c) Logic Design d) Circuit Design e) Physical Design	**10**	**CO1**
	SECTION-C		
Q9	a) Design the synchronous sequential circuit for the following state graph. Choose flip-flop of your choice b) Write the VHDL code for the design using dataflow model c) Write the Verilog code for the design using structural model 	**20**	**CO4**
Q10	Analyze the following multiplexer VHDL code carefully and write the simulation test bench for the same with neat graph. And make the necessary changes to the code to make it synthesizable on FPGA. **architecture Behavioral of mux is** **begin** **process(a, sel) is** **begin** **if(sel(0)<='0' and sel(1)<='0') then y<=a(0);** **elsif(sel(0)<='1' and sel(1)<='0') then y<=a(1);** **elsif(sel(0)<='0' and sel(1)<='1') then y<=a(2);** **elsif(sel(0)<='1' and sel(1)<='1') then y<=a(3);** **end if;** **end process;**	**20**	**CO2**

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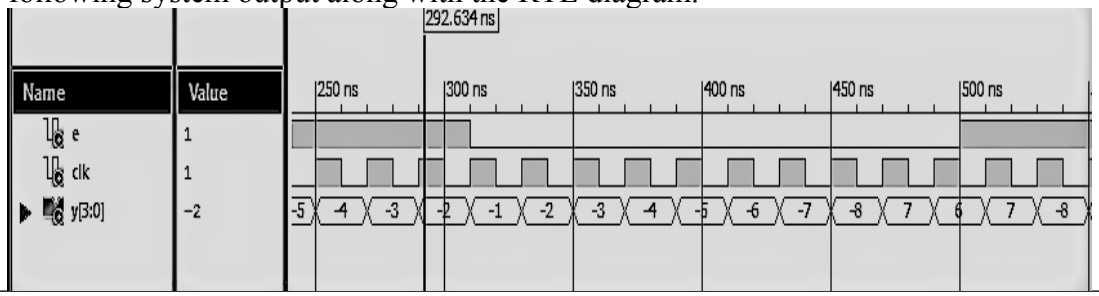
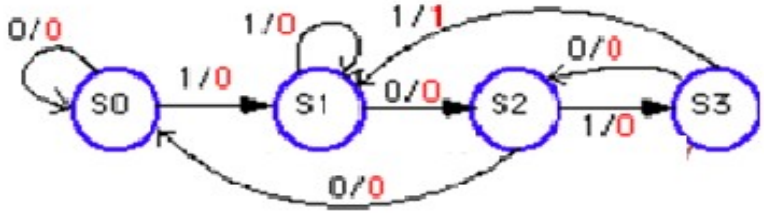
SECTION A

S. No.		Marks	CO
Q 1	List out atleast ten different keywords in VHDL and Verilog HDL's. And also differentiate between ASIC and FPGA design.	**5**	**CO3**
Q2	Explain the Gajski's Y-chart system to silicon level VLSI Design with neat sketch.	**5**	**CO1**
Q3	Construct the basic layout of SPLD architecture with neat sketch.	**5**	**CO2**
Q4	Write the Verilog code and the stimulus for the following Boolean function x = A + BC + B'D y = B'C + BC'D'	**5**	**CO4**
	SECTION B		
Q5	Mention all the types of pre-defined data types, operators and data & signal attributes in VHDL. And also Mention the output for the following. i. W <= (0 =>'1', OTHERS => '0'); ii. d'Reverse_range of **Signal d:std_logic_vector(7 downto 0);** iii. If x<="1001010" then Y<= x sra 4	**10**	**CO1**
Q6	Observe the following graph carefully, derive the specifications of the system, create the logic, generate the complete VHDL code and the test bench required to get the following system output along with the RTL diagram. 	**10**	**CO3**
Q7	Develop 4-bit, 2's complement adder/subtractor using Full adder as component. The control line M='1' performs subtraction and M='0' performs addition.	**10**	**CO3**
Q8	Analyze the following design terms in the VLSI design cycle a) Architectural Design b) Functional Design c) Logic Design d) Circuit Design e) Physical Design	**10**	**CO1**
	SECTION C		
Q8	a) Design the synchronous sequential circuit for the following state graph. Choose flip-flop of your choice b) Write the VHDL code for the design using dataflow model	**20**	**CO4**

	c) Write the Verilog code for the design using structural model  		
Q10	Analyze the following Decoder VHDL code carefully, insert ICON, ILA and VIO IP cores into the code to implement the same on FPGA hardware. **entity decoder is** **port(** **a : in STD_LOGIC_VECTOR(1 downto 0);** **b : out STD_LOGIC_VECTOR(3 downto 0));** **end decoder;** **architecture bhv of decoder is** **begin** **process(a)** **begin** **case a is** **when "00" => b <= "0001"; when "01" => b <= "0010"; when "10" => b <= "0100";** **when "11" => b <= "1000";** **end case;** **end process;** **end bhv;**	**20**	**CO2**

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