Name: **Enrolment No:**	

UPES

End Semester Examination, May 2025

Course: Digital System Design

Semester: IV

Program: B.TECH Electronics and Computer Engg./Electrical Engg. **Time : 03 hrs.**

Course Code: ECEG2070 **Max. Marks: 100**

Instructions: • **Read all questions carefully before answering.**

Answer all questions in the order they are given.

Keep answers to the point and avoid unnecessary details.

Keep your handwriting neat.

Manage your time to complete all questions.

SECTION A
(5Qx4M=20Marks)

S. No.		Marks	CO
Q 1	Explain the working of a NAND Latch (Active Low S-R) with a suitable diagram.	**4**	**CO1**
Q2	What is meant by state reduction? What is the lock-out condition in sequential circuits, and how can it be resolved? Illustrate with a simple example.	**4**	**CO2**
Q3	List the components of an ASM chart. Why is it considered more efficient than a conventional state diagram?	**4**	**CO3**
Q4	What are the major issues associated with asynchronous circuit design? Describe the different methods used in asynchronous design.	**4**	**CO3**
Q5	Draw a TTL NAND gate and explain its operation with the help of a truth table.	**4**	**CO4**

SECTION B
(4Qx10M= 40 Marks)

Q6	Design and implement a sequence generator that goes through states **0, 1, 2, 4, 0** using **D flip-flops**. The unused states must go to zero **(000)** on the next state. Based on the given state transition table, derive the excitation equations for each flip-flop and build the logic circuit. Use Boolean algebra or Karnaugh maps to simplify the equations and then implement the design using appropriate logic gates.	**10**	**CO2**

Q7	Apply the concept of ASM chart design to construct an ASM chart for a Mod-4 Up-Down counter. Clearly show state transitions based on the control input (Up/Down) and represent the counter's behavior using appropriate ASM elements.	**10**	**CO3**
Q8	Design a Mod-12 asynchronous up counter using JK flip-flops. Apply the CLEAR input strategically to reset the counter when the count reaches decimal 12. Show the logic circuit diagram, explain the reset condition, and justify your choice of flip-flop configuration.	**10**	**CO1**
Q9	Implement a 3-input NAND gate and a 2-input XOR gate using CMOS logic. Evaluate the ON/OFF status of all PMOS and NMOS transistors for all input combinations.	**10**	**CO4**
SECTION-C (2Qx20M=40 Marks)			
Q 10	a. Design and create a sequence generator using J- K flip-flops that generates the sequence **0 → 2 → 4 → 5 → 1 → 7 → 6 → 0.** Derive the state transition diagram and table for the given sequence. Formulate the excitation equations for each J-K flip-flop based on the state transitions and simplify the Boolean expressions using Karnaugh maps or Boolean algebra. Construct the logic circuit using J-K flip-flops and the appropriate logic gates based on your simplified equations. b. Write a short note on PAL and PLA. A combinational circuit is defined by the functions: **$f_1 = \sum m(3,5,7)$, $f_2 = \sum m(4,5,7)$** Implement the circuit with a PLA having 3 inputs, 3 product terms and two outputs.	**10+10**	**CO2, CO4**
11	a. For the clocked sequential circuit given below (**Figure 1**) derive the input and output equations. Using these equations, determine the next-state equations for each state variable. Construct the present state table and next state table. Finally, draw the state diagram to represent the behavior of the circuit. (D flip flops are used)	**15+5**	**CO2, CO4**

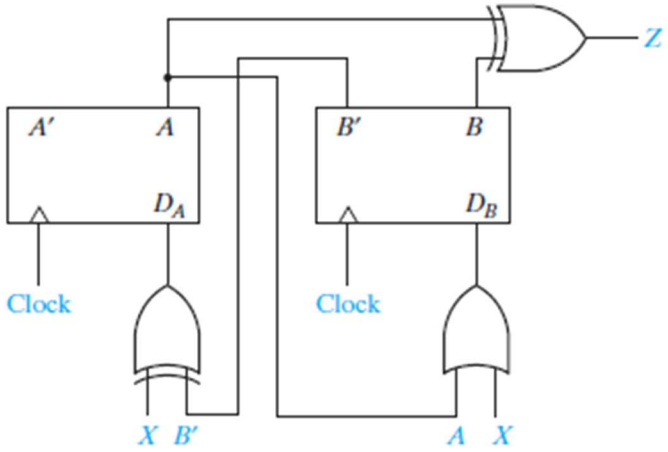

Figure 1

b. Write a short note on FPGA Based Design.

OR

a. You are given a finite state machine (FSM) in **figure 2** with 6 states labeled using 3-bit binary values and transitions based on 1-bit input (X) producing a 1-bit output (Z). Design a hardware implementation of this FSM using **T flip-flops and basic gates**.

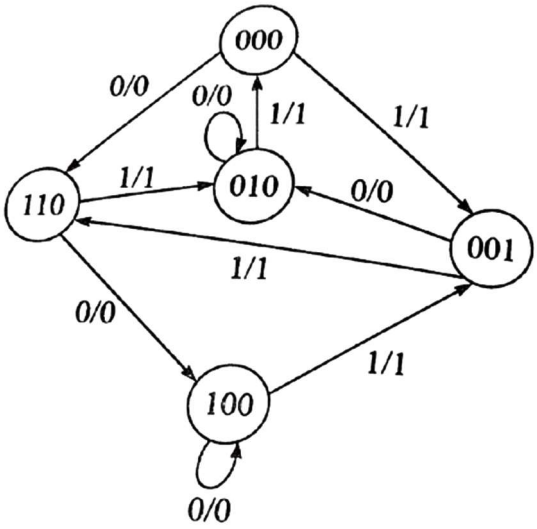

Figure 2

	b. Write a short note on Noise Margin and Power Dissipation (with respect to digital ICs)		