Name: **Enrolment No:**	

UNIVERSITY OF PETROLEUM AND ENERGY STUDIES
End Semester Examination, May 2025

Course: Analog Electronics-I — Semester: II
Program: B. Tech. (Electronics and Computer Engineering & Electrical Engineering). — Time: 3 hrs
Course Code: ECEG 1014. — Max. Marks: 100

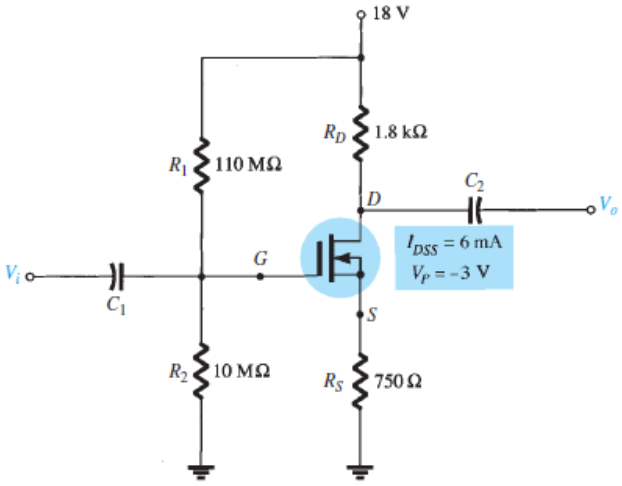
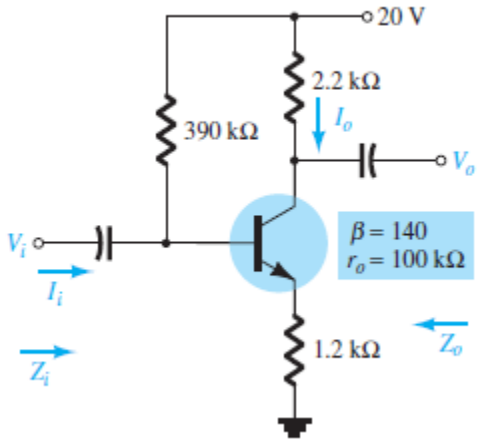
Instructions: The QP is 2 pages long. Draw the neat and clean diagram wherever it is needed. **Graph sheets will be provided in the examination hall.**

SECTION A

S. No.		Marks	CO
Q 1	Given that the DC current gain β_{dc}=150 and the collector current I_C=3.0 mA, calculate the emitter current I_E and the base current I_B	**4**	**CO1**
Q 2	Draw the basic construction of an n-channel D-MOSFET. What is the effect of V_{GS} on channel width?	**4**	**CO1**
Q 3	Compare Field Effect Transistors' (FET) advantages and disadvantages to those of BJTs.	**4**	**CO1**
Q 4	Plot the frequency response curve of a BJT amplifier and clearly indicate the lower and upper cutoff frequencies on the graph. Additionally, define what is meant by the lower and upper cutoff frequencies.	**4**	**CO3**
Q 5	An n-channel JFET has the following device parameters: I_{DSS} = 8 mA and pinch-off voltage V_P = − 4 V. Plot the transfer characteristics using the provided graph paper.	**4**	**CO2**

SECTION B

Q 6	Draw the high-frequency equivalent circuit (Hybrid-π model) of a Bipolar Junction Transistor (BJT) configured in Common Emitter (CE) mode. Clearly label all the components in the model. Explain the physical origin and significance of each component that appears in the equivalent circuit	**10**	**CO3**
Q 7	Three identical amplifier stages are cascaded, and the overall system exhibits a lower 3-dB frequency of 20 Hz and an upper 3-dB frequency of 20 kHz. Assuming that the stages are non-interacting, determine the lower cutoff frequency f_L and upper cutoff frequency f_H for each individual stage.	**10**	**CO4**
Q 8	Describe the construction and working principle of an n-channel Junction Field Effect Transistor (JFET). Sketch and explain its drain characteristics in detail. Also, draw the standard circuit symbol for an n-channel or p-channel JFET.	**10**	**CO1**
Q 9	An enhancement-type n-channel MOSFET has the following parameters: • $V_{GS(ON)}$ = 6V and $I_{D(ON)}$ = 4mA. • Threshold voltage V_T= +2 V Calculate the drain current I_D for the following values of gate-to-source voltage V_{GS}	**10**	**CO2**

	(a) $V_{GS} = 0$ V (b) $V_{GS} = +2$ V (c) $V_{GS} = +4$ V (d) + 8V		
	SECTION-C		
Q 10	For the n-channel depletion-type MOSFET of below figure, determine: (i) I_{DQ} and V_{GSQ} (ii) V_{DSQ}, (iii) Z_i, (iv) Z_o, and (v) A_v. (Hint: Do both DC and AC analysis and use the graph to calculate the V_{GSQ}) 	**20**	**CO3**
Q 11	(a) Draw the circuit diagram of a Darlington pair configured as an emitter follower. Clearly label all components and voltages. (b) Derive expressions for the overall input impedance, output impedance, and voltage gain of the Darlington emitter follower. Compare them with a single transistor emitter follower. **OR** For the network of the following figure: (a) Determine $I_{BQ}, I_{CQ}, V_{CEQ}, and\ r_e$. (b) Find Z_i and Z_o. (c) Calculate A_v 	**5+15** **20**	**CO4** **CO3**