Name: **Enrolment No:**	UPES UNIVERSITY OF TOMORROW

UPES

End Semester Examination, May 2024

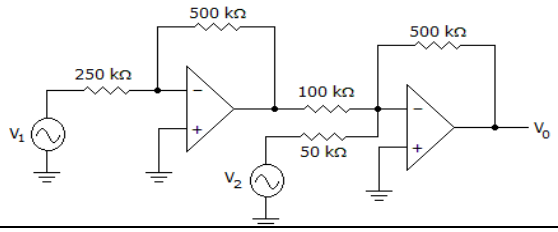
Course: Analog and Digital Electronics — **Semester: IV**

Program: B. Tech Mechatronics — **Time : 03 hrs.**

Course Code: ECEG-2030 — **Max. Marks: 100**

SECTION A

(5Qx4M=20Marks)

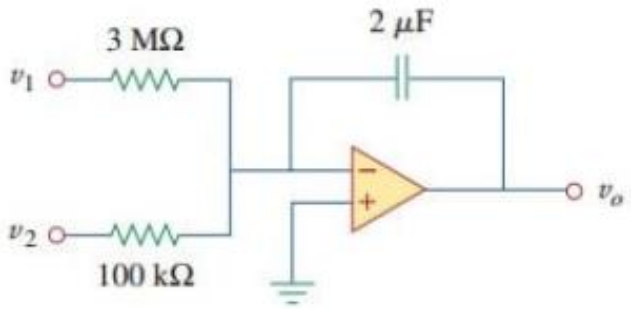
S. No.	**Attempt all the questions.**	**Marks**	**CO**
Q 1	An op-amp has a CMRR of 90 dB. If the common-mode gain is 0.01, calculate the differential gain.	**4**	**CO2**
Q 2	Convert the following: i. $(101100111)_{BCD}$ to Excess-3 code ii. $(101100.1100)_{Gray\ Code}$ to Binary	**4**	**CO1**
Q 3	Calculate the output voltage if V_1 = 300 mV and V_2 = 700 mV. 	**4**	**CO2**
Q 4	Describe the inverting and non-inverting op-amp using suitable configuration and derive the gain expression.	**4**	**CO1**
Q 5	Simplify the Boolean function: $F(w, x, y) = \pi\ (1, 3, 4, 7)$ that has the don't-care conditions $d(w, x, y) = \sum\ (0, 2, 5)$	**4**	**CO3**

SECTION B

(4Qx10M= 40 Marks)

Answer any four questions

Q 6	Compare and contrast voltage feedback and current feedback configurations in amplifier circuits.	**10**	**CO3**
Q 7	Describe the internal block diagram and operation of the 555 timer IC. Explain how it can be configured as an astable multivibrator.	**10**	**CO2**
Q 8	Determine the values of Current gain A_I, Ri, Voltage gain Av and Yo for a Common base configuration circuit, if the h-parameters are hfb = -0.95; hob= 0.45μA/V ; hib= 21. Ω; hrb = 2.9×10^{-6};Ri=Rs=1KΩ; R_L=10KΩ.	**10**	**CO4**
Q 9	Design a 4-bit Synchronous UP counter using JK flip flop and write down the steps involved in the designing process.	**10**	**CO4**

Q10	Design a 4-bit ring counter using D flip-flops and explain the change in cycles through its states. Discuss the applications of ring counters in digital systems.	**10**	**CO4**
SECTION-C (2Qx20M=40 Marks) **Answer any two questions**			
Q 11	a. Design a JK flip-flop using SR flip flop. Also, derive the expression for the excitation table. b. Implement the 3-input full subtractor circuit using logic gates.	**15+5**	**CO4**
Q 12	a. Design and explain the operation of SIPO shift register. b. Design a sequence generator with the following sequence: 0-2-5-4-7.	**10+10**	**CO4**
Q 13	a. Design a 4- bit Parallel adder circuit using suitable diagram. b. Calculate the output voltage of the given integrator Op-Amp. 	**10+10**	**CO4**