Name: **Enrolment No:**	

UPES

End Semester Examination, May 2024

Course: Computer Organization & Architecture **Semester: IV**

Program: B. Tech. (Electronics & Computer Engineering) **Time: 03 hrs.**

Course Code: CSEG 2044 **Max. Marks: 100**

Instructions: Attempt all the questions.

SECTION A
(5Qx4M=20Marks)

S. No.		Marks	CO
Q 1	Differentiate RISC and CISC architecture.	**4**	**CO1**
Q 2	Design D flip-flop using J-K flip flop.	**4**	**CO2**
Q 3	Elucidate the significance of control unit in a digital computer. List its important functions while execution of assembly language program.	**4**	**CO3**
Q 4	Differentiate strobe control and handshaking asynchronous data transfer techniques.	**4**	**CO4**
Q 5	Design and implement 3 to 8 line decoder circuit.	**4**	**CO2**

SECTION B
(4Qx10M= 40 Marks)

Q 6	Elucidate the significance of following instructions: (a) LDA (b) CLA (c) BSA (d) ION (e) SKI (f) EI (g) SHR (h) RET (i) CMP (j) TST	**10**	**CO1**
Q 7	Design a sequence generator using D flip-flop to generate the sequence 101100110.	**10**	**CO2**
Q 8	Explain microinstruction format and discuss the significance of each field. Write the symbolic microprogram for fetch routine in assembly language.	**10**	**CO3**

Q 9	Explain associative memory with the help of a suitable block diagram. Give a suitable example explaining how the argument data is searched within the associative memory. **OR** What do understand by direct memory access (DMA)? Explain DMA controller with suitable block diagram.	**10**	**CO4**
SECTION-C (2Qx20M=40 Marks)			
Q 10	(a) What do you understand by pipelining? In certain scientific computations it is necessary to perform arithmetic operation $(A_i + B_i) * (C_i + D_i)$ with a stream of numbers. Specify a pipeline configuration to carry out the task. List the contents of all registers in the pipeline for $i = 1\ through\ 6$. (b) Design and explain hardwired control unit of a digital computer. **OR** (a) Differentiate arithmetic pipeline and instruction pipeline. Design a arithmetic pipeline for floating-point subtraction of two numbers: $X = 0.3235\ X\ 10^3$ $Y = 0.2365\ X\ 10^2$ Explain the pipelining operation with the help of flow-chart. (b) Explain address sequencing for control memory in microprogrammed control unit with a suitable diagram.	**20**	**CO3**
Q 11	(a) A computer employs RAM chips of 256 X 8 and ROM chips of 1024 X 8. The computer system needs 2K bytes of RAM, 2K bytes of ROM. (i) How many RAM and ROM chips are needed? (ii) Draw a memory-address map for the system. (iii) Give the address range in hexadecimal for RAM and ROM. (b) A 4-way set associative cache memory unit with a capacity of 16 KB is built using a block size of 8 words. The word length is 32 bits. The size of the physical address space is 4 GB. What are the number of bits for the TAG field?	**20**	**CO4**