Name: **Enrolment No:**	

UPES

End Semester Examination, May, 2024

Program Name: B.Tech Electrical Engineering/ Electronics & Computer Engineering **Semester: II**

Course Name: Digital Logic & Computer Architecture **Time: 3 hrs**

Course Code: CSEG-1015 **Max. Marks: 100**

Nos. of page(s): 2

Instructions: Assume any data in the design, if required.

SECTION-A (5Q x 4M = 20 Marks)

S. No.		Marks	CO
Q.1	List the different features of Register transfer language (RTL) in computer organization.	**4**	**CO1**
Q.2	(a) Implement the XOR using NOR (b) Implement the XOR using NAND	**2+2**	**CO2**
Q.3	Given the two binary numbers X = 1010100 and Y = 1000011, perform the subtraction (a) X - Y and (b) Y - X by using 2's complements.	**4**	**CO1**
Q.4	Draw the system bus architecture in computer organization. A RAM chip has a size (8Kx16) then determine. (a) No of address lines (b) No of data lines (c) No of possible registers (d) No of flip-flops	**4**	**CO2**
Q.5	(a) State and prove Demorgan's Theorem using the truth table. (b) Prove the associative law: A + (B + C) = (A + B) + C	**2+2**	**CO1**

SECTION B (4Q x 10M = 40 Marks)

Attempt all of the followings

Q.6	What are the microoperations of a processor? Explain arithmetic microoperations. ***OR*** Discuss Flynn's taxonomy for computer architecture. Compare RISC and CISC architecture.	**10**	**CO1**
Q.7	Explain the functionality of the (3x8) decoder with a complete truth table, equations, and logic diagram.	**10**	**CO2**
Q.8	Discuss the IEEE floating point format for 8-bit, 16-bit, 32-bit, and 64-bit. Convert number $(85.125)_{10}$ to 16-bit and 32-bit IEEE format.	**10**	**CO4**
Q.9	(a) Detail the working of (1x4) demultiplexer with logic diagram, equation, and truth table. (b) Detailed the working of a 3-bit error generator and 4-bit error detection circuit with logic diagram, equation, and truth table.	**10**	**CO3**

SECTION-C (2Q x 20M = 40 Marks)

Attempt any *two of* the following

Q.10	**(a)** Explain the detailed concept of RAM and ROM Chips and pins. How are memory connections taken to the CPU? Take an example of memory interface to CPU. Take an example of the memory interface chips listed below. Detail the functionality of the design and interface. **(b)** Explain the detailed working and diagram of NMOS-based dynamic RAM.	**10+10**	**CO4**
Q.11	**(a)** Design a code converter that accepts BCD inputs and converts them to its equivalent excess-3 code. **(b)** How the full adder operation is performed using two half adders. Design a look ahead carry adder/generator (4-bit). Detail the complete description with equations, logic diagram, and truth table.	**10+10**	**CO2**
Q.12	**(a)** Explain the different operations of Arithmetic and logical unit (ALU) in detail. Let A= 78 H and B= 81 H and we want to perform the addition Show the status of all the status registers in ALU. **(b)** Simplify the Boolean functions using K-Map **F (w, x, y, z) = ∑m (0, 1, 2, 4, 5, 6, 7, 10, 15)** **F (A, B, C, D) = πM (1, 3, 5, 7, 13, 15)**	**10+10**	**CO3**

Component	Hexa address	Address bus									
		10	9	8	7	6	5	4	3	2	1
RAM 1	0000 - 007F	0	0	0	x	x	x	x	x	x	x
RAM 2	0080 - 00FF	0	0	1	x	x	x	x	x	x	x
RAM 3	0100 - 017F	0	1	0	x	x	x	x	x	x	x
RAM 4	0180 - 01FF	0	1	1	x	x	x	x	x	x	x
ROM	0200 - 03FF	1	x	x	x	x	x	x	x	x	x