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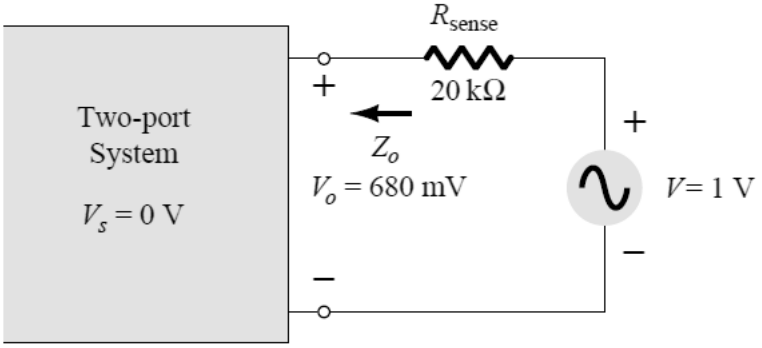
| **Name:**<br>**Enrolment No:** | |

# UPES

**End Semester Examination, December, 2023**

**Programme Name: B Tech– Electronics and Communication Engineering** **Semester : III**
**Course Name : Analog Electronics-I** **Time : 3 hr**
**Course Code : ECEG-2011** **Max. Marks: 100**
**Nos. of page(s) : 03**
**Instructions: Attempt all the sections.**

**SECTION A (5Qx4M=20Marks)**

| S. No. | **Attempt all the questions.** | **Marks** | **CO** |
|---|---|---|---|
| Q 1 | Defend the physical significance of operating point (Q) location on DC load line of Bipolar Junction Transistor (BJT). Show the optimal position of Q through DC load line and what will be the effect on the performance of transistor based amplifier if Q deviates from its original position. | **4** | **CO1** |
| Q2 | For the system of Fig. (1), determine the level of output impedance.<br>  <br><br>Fig. (1) | **4** | **CO1** |
| Q3 | Sketch and analyze the transconductance curve which gives us the relationship between drain current $(I_D)$ and gate-to-source voltage$(V_{GS})$. | **4** | **CO2** |
| Q4 | Define the terms for Junction field effect transistor (JFET),<br>(a) A. C. drain resistance $(r_d)$<br>(b) Amplification factor (μ)<br>(c) Input resistance $(R_i)$ | **2+1+1** | **CO3** |
| Q5 | Write the overall gain 'A' of the three-stage operation amplifier as connected in the series connection.<br>***Note:*** First op-amp is Non-inverting and rest two op-amps are inverting. Draw the connection diagram also. | **4** | **CO4** |

| SECTION B (4Qx10M= 40 Marks) | | | |
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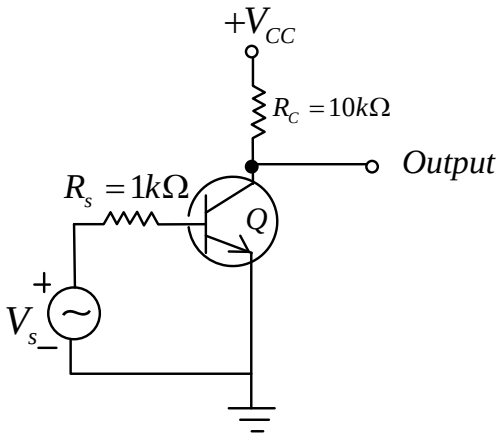
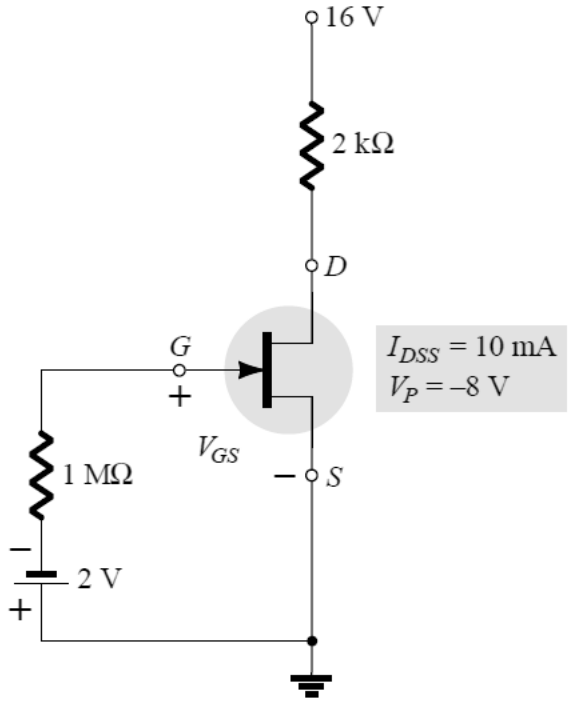
| Q 6 | For the CE amplifier shown in Fig. (2), following data are given:<br>$h_{ie} = 1.1k\Omega, \quad h_{re} = 1.5 \times 10^{-4}, \quad h_{fe} = 50, \quad h_{oe} = 24\mu A/V.$<br>Calculate: $A_i$, $A_v$, $R_i$, $A_{is}$ and $A_{vs}$ for $R_L = 10\ k\Omega$.<br>  <br><br>Fig. (2) | **10** | **CO1** |
| Q7 | Compare Junction field effect transistor (JFET) and Metal oxide semiconductor field effect transistor (MOSFET).<br>An N-channel JFET has $I_{DSS} = 8mA$ and $V_P = -5V$. Find the minimum value of $V_{DS}$ for pinch-off region and the drain current $I_{DS}$, for $V_{GS} = -2V$ in the pinch-off region. | **10** | **CO2** |
| Q8 | Determine the following for the network of Fig. (3),<br>(a) $V_{GSQ}$ (b) $I_{DQ}$ (c) $V_{DS}$ (d) $V_D$ (e) $V_G$ (f) $V_S$<br>  <br><br>**Fig. (3)** | **10** | **CO3** |

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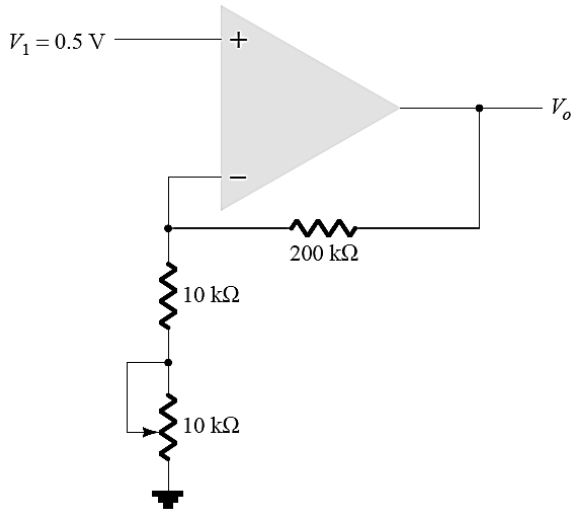
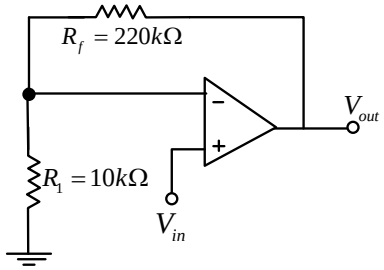
| Q9 | Derive the expression of voltage gain for inverting operation amplifier. What will be range of voltage gain for the given operation amplifier circuit as shown in Fig. (4).<br>  <br><br>**Fig. (4)** | **10** | **CO4** |
| **SECTION-C (2Qx20M=40 Marks)** | | | |
| Q 10 | **(a)** Determine the input and output impedances of the amplifier in Fig. (5). The op-amp data sheet gives $Z_{in=}2M\Omega$ , $Z_{out=}75\Omega$ and open loop gain of 200,000. Also determine the closed voltage gain and feedback fraction.<br>  <br><br>Fig. (5)<br>**(b)** Show the connection of three op-amp stages using an LM348 IC to provide outputs that are 10, 20, and 50 times larger than the input. Use a feedback resistor of $R_f$ =500 kΩ in all stages. | **10+10** | **CO3** |
| Q11 | **(a)** Show the connection of an LM124 quad op-amp as a three-stage amplifier with gains of +10, -18, and -27. Use a 270kΩ feedback resistor for all three circuits. What output voltage will result for an input of 150 μV?<br>**(b)** Design and analyze the following any two applications of operation amplifier,<br>(i) Averaging operation amplifier<br>(ii) Substractor operation amplifier<br>(iii) Integrator operation amplifier | **10+10** | **CO4** |