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UPES

UNIVERSITY OF PETROLEUM AND ENERGY STUDIES

End Semester Examination, December 2017

Program: B Tech (EE, EE-BCT) | **Semester – III**
Subject (Course): Electronic Devices and Circuits-I | **Max. Marks : 100**
Course Code: ELEG218 | **Duration : 3 Hrs**
No. of page/s: 3

Instructions:

- Attempt all questions.
- There is an internal choice for Q.No- (9) and (11) (i.e. attempt only one part of these question either (a) or (b))
- Assume any data if required and indicate the same clearly. Unless otherwise indicated symbols and notations have their usual meanings.
- Strike off all unused blank pages

Section-A (5x4 = 20 Marks)

1. Describe the conditions established by forward- and reverse-bias conditions on a *p–n* junction diode and how the resulting current is affected.
2. Find the intrinsic carrier concentration of Germanium, if its intrinsic resistivity at 300 °K is 0.47 ohm-m. It is given that the electronic charge is 1.6 x 10^{-19}coulombs, and that electron and hole mobilities at 300 °K are 0.39 and 0.19 m^2/(V.sec)
3. List the three sources of instability of collector current in BJT. Define three stability factors.
4. The leakage currents of a transistor, with usual notations, are I_{CEO} = 410 µA and I_{CBO} = 5µA, the base current I_B being 30 µA. Calculate the collector current.
5. Give reasons why MOSFETs dominate in VLSI over BJT.

Section-B (4x10 = 40 Marks)

6. **(a)** A half wave rectifier having a diode with an internal resistance of 50 Ω is to supply power to a 1 kΩ load from 110 V rms source of supply, calculate peak load current; dc load current; dc diode voltage; ac load current
   (b) A 5.2 V Zener diode has a maximum power dissipation of 260 mW. It maintains a constant voltage when the current though the diode does not fall below 10% of the maximum permissible currents. A 15 V supply is given to the Zener through a series resistor R. Find the range for R so that the Zener maintains its constant voltage. Find the new range when the diode is loaded by 50 Ω load.
7. Define stabilization technique and compensation techniques to maintain the operating point of transistor in active region. Also explain diode compensation technique for V_{BE}
8. Explain the basic construction and operation of JFET.

9. **(a)** For the circuit shown in **Fig. 1**, find the labeled node voltages for: (a) $\beta = \infty$ (b) $\beta = 100$

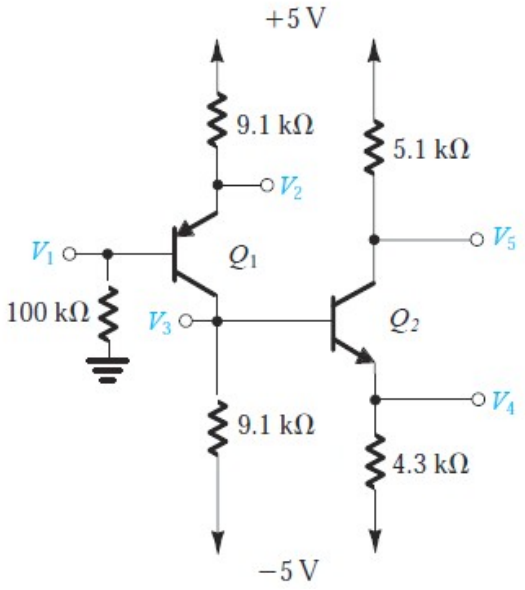

Fig. 1

Or

(b) Consider an npn transistor for which $\beta_F = 100$, $\alpha_R = 0.1$, and $I_S = 10^{-15}$ A.

(i) If the transistor is operated in the forward active mode with $I_B = 10$ μA and $V_{CB} = 1$ V, find V_{BE}, I_C, and I_E

(ii) Now, operate the transistor in the reverse active mode with a forward-bias voltage V_{BC} equal to the value of V_{BE} found in **(i)** and with $V_{EB} = 1$ V. Find I_C, I_B, and I_E

Section-C (2x20=40 Marks)

10. **(a)** Design a circuit using two diodes, one resistor and two voltage sources that would convert the input signal (V_{in}) to the output voltage (V_{out}) as shown in **Fig. 2** the resistor value need not be specified.

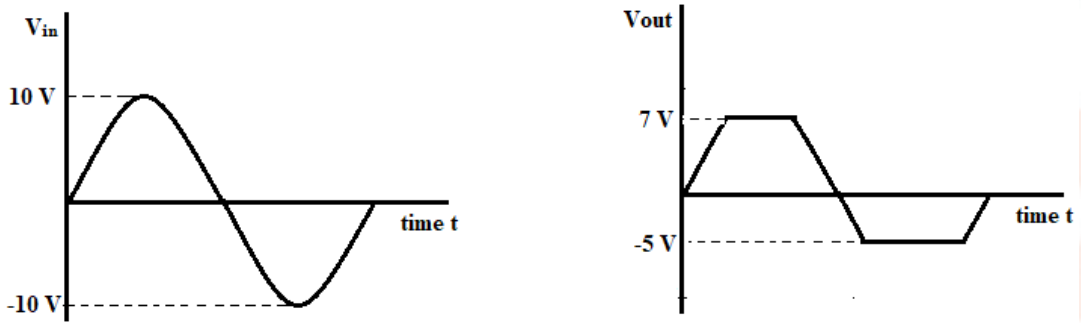

Fig. 2

(b) Design a voltage-divider bias network shown in **Fig. 3** using a depletion-type MOSFET with $I_{DSS} = 8$ mA and $V_P = -¿\ 3$ V to have a Q -point at $I_{DQ} = 2.5$ mA using a supply of 20 V. In addition, set $V_G = 4$ V and use $R_D = 8R_S$ with $R_2 = 10$ MΩ

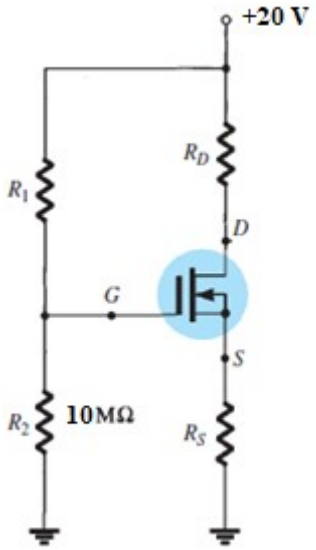

Fig. 3

11. **(a)** It is required to design the circuit in **Fig. 4** so that a current of 1 mA is established in the emitter and a voltage of +5 V appears at the collector. The transistor type used has a nominal β of 100. However, the βvalue can be as low as 50 and as high as 150. Your design should ensure that the specified emitter current is obtained when β = 100 and that at the extreme values of β the emitter current does not change by more than 10% of its nominal value.

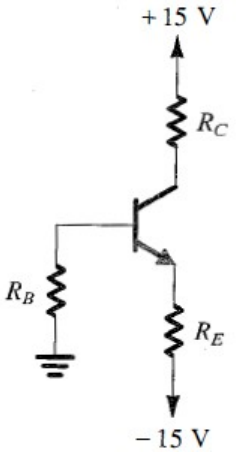

Fig. 4

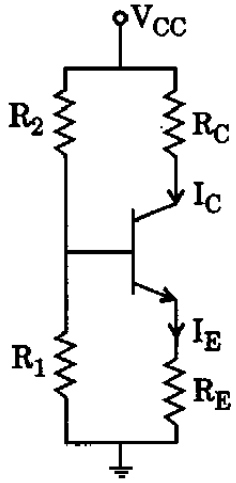

Fig. 5

Or

(b) Design a self-biasing circuit shown in **Fig. 5** such that $V_{CC} = 8$ V, $I_C = 5$ mA, $V_E = 6$ V, β = 200 and stability factor S = 10.

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Section-A (4x5 = 20 Marks)

1. The intrinsic resistivity of germanium at 300 K is 47 ohm-cm. What is its intrinsic carrier concentration? Also, calculate the drift velocity of holes and of electrons for an electric field E = 100 V/cm. Given : $\mu_n = 0 = 3.9\ m^2/V$ sec and $\mu_p = 0.19\ m^2/V$ sec. (Electronic chare q = 1.6×10^{-19} C)
2. Describe how you will remember the forward- and reverse-bias states of the *p – n* junction diode. That is, how will you remember which potential (positive or negative) is applied to which terminal?
3. Discuss the thermal runaway in BJTs.
4. Explain in your own words why the application of a positive voltage to the gate of an *n* –channel depletion-type MOSFET will result in a drain current exceeding I_{DSS}.

Section-B (4x10 = 40 Marks)

5. For the circuits shown in **Fig. 1** and **Fig. 2**, sketch and explain the output waveforms. Assume the diodes are ideal.

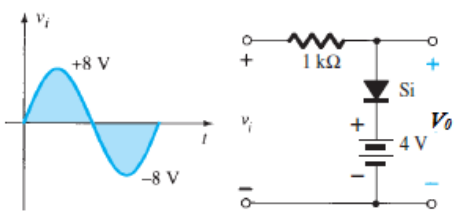

Fig.1

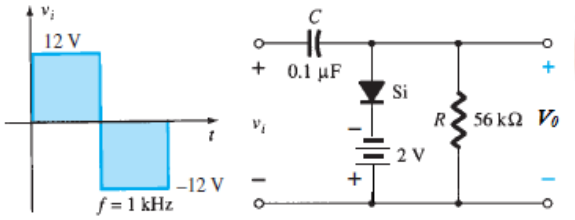

Fig. 2

6. Sketch and explain the output V-I characteristics of an NPN transistor in common-emitter operation and indicate there on the different regions of importance.
7. What do you mean by 'saturation' of a transistor? In the circuit shown in **Fig. 2**, determine V_{BB} to saturate the transistor. Assume V_{CEsat} = 0.1 V, $V_{E,sat}$ = 0.6 V and β = 50.

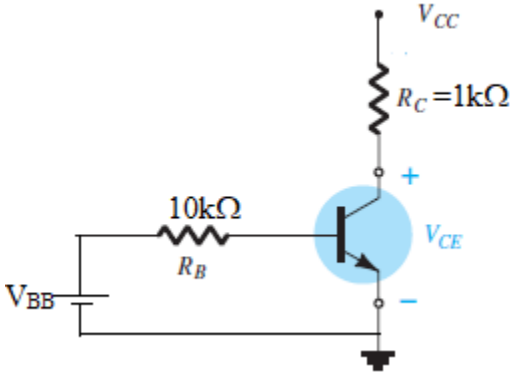

Fig. 2

8. Draw and explain the drain and transfer characteristics of a n-channel enhancement type MOSFET. What is meant by threshold voltage? Discuss three different ways by which the threshold voltage can be reduced.

Section-C (2x20=40 Marks)

9. Consider the two-supply bias arrangement shown in **Fig. 3** using ±3 V supplies. It is required to design the circuit so that I_C = 3 mA and V_C is placed midway between V_{CC} and V_E.
   (a) For $\beta = \infty$, what values of R_E and R_C are required?
   (b) If the BIT is specified to have a minimum β of 90, find the largest value for R_B consistent with the need to limit the voltage drop across it to one-tenth the voltage drop across R_E.

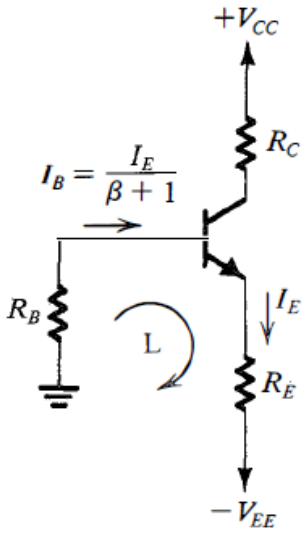

Fig. 3

10. (a) A simple full wave bridge rectifier circuit has an input voltage of 240 V a.c. r.m.s. Assume the diodes to be ideal. Find the output d.c. current, d.c. voltage, r.m.s. values of output currents and voltages and the peak inverse voltage that appears across the non- conducting diode. Assume load resistance to be 10kΩ.
(b) Design the circuit of **Fig. 4** to establish a drain current of 0.25 mA and a drain voltage of 0 V. The MOSFET has $V_T = 1$ V, $\mu_n C_{ox} = 60\ \mu A/V^2$, $L = 3\ \mu m$, and $W = 100\ \mu m$.

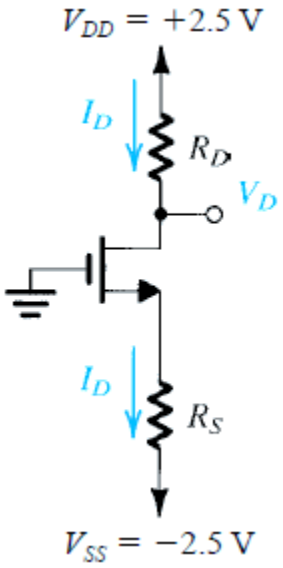

Fig. 4