

## UNIVERSITY OF PETROLEUM AND ENERGY STUDIES

End Semester Examination, December 2017

Program: B.Tech ASEA

Subject (Course): DIGITAL ELECTRONICS

Course Code : ELEG 220

No. of page/s: 02

Semester – III

Max. Marks : 100

Duration : 3 Hrs

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### Sec(A)

All questions are compulsory and each carry 5 marks.

1. What are the four types of flip-flop?
2. Why must the T and JK flip-flops be clocked.
3. In what ways can the operation of a flip-flop be described .
4. Differentiate between synchronous and asynchronous inputs.

### Sec(B)

All questions are compulsory and each carry 10 marks.

5. In general how many flip-flops are required to produce a mod-N counter, how many unused states will there be, and what is the outcome of entering these 'unused states'?
6. A four-bit ring counter and a four-bit Johnson counter are in turn clocked by a 10 MHz clock signal. Determine the frequency and duty cycle of the output of the output flip-flop in the two cases.
7. Draw the function table for (a) a negative edge-triggered D flip-flop and (b) a D latch with an active LOW ENABLE input.
8. Differentiate between:
  - a. synchronous and asynchronous inputs;
  - b. level-triggered and edge-triggered flip-flops;
  - c. active LOW and active HIGH inputs.

**Sec(C)**

**All questions are compulsory and each carry 20 marks.**

9. Design a mod-N counter, how many unused states will there be, and what is the outcome of entering these 'unused states'? What is the procedure for producing an asynchronous binary mod-N counter, and what problems may be encountered when using such a circuit in practice?
  
10. Design a combinational circuit which is defined by  $F = \Sigma 0, 2, 5, 6, 7$ . Hardware implement the Boolean function F with a suitable decoder and an external OR/NOR gate having the minimum number of inputs.

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### Sec(A)

All questions are compulsory and each carry 5 marks.

1. What do the terms level triggered and edge triggered mean? (CO1)
2. What is a shift register, and why can such a circuit be used to multiply a binary number by 2". (CO3)
3. What is the 'mod' of a counter? (CO4)
4. What do the terms preset and reset mean when referred to counters? (CO4)

### Sec(B)

All questions are compulsory and each carry 10 marks.

5. Draw the truth table for the following types of flip-flop: (CO3)
  - a) a positive edge-triggered J-K flip-flop with active HIGH J and K inputs and active LOW PRESET and CLEAR inputs;
  - b) a negative edge-triggered J-K flip-flop with active LOW J and K inputs and active LOW PRESET and CLEAR inputs.
6. Briefly describe the following flip-flop timing parameters: (CO2)
  - (a) set-up time and hold time;
  - (b) propagation delay;
  - (c) maximum clock frequency.
7. What is meant by the race problem in flip-flops? How does a master–slave configuration help in solving this problem?

8. What does the circuit in Fig. 1 do? (CO3)

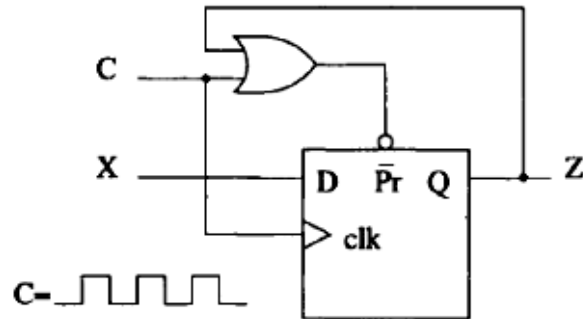
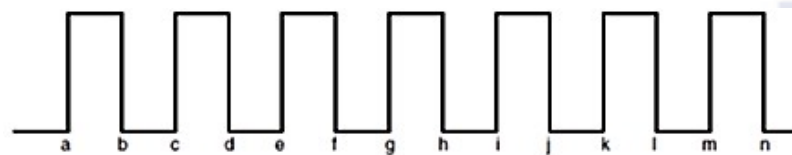


Fig. 1

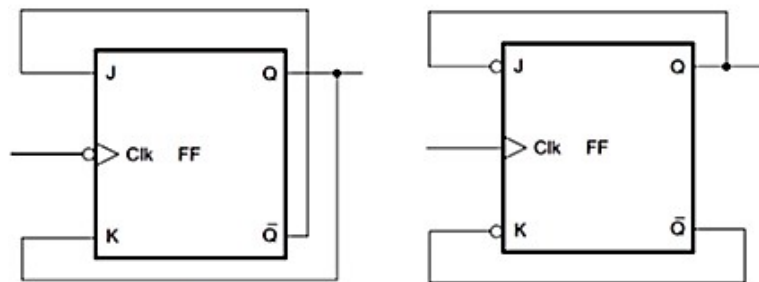
Sec(C)

All questions are compulsory and each carry 20 marks.

9. Design a mod-7 synchronous binary counter using JK flip-flops. Determine what happens if the count goes into any of the unused states and show the results on a state diagram. How must the circuit be modified if the unused state is to lead to state 4 (i.e. outputs of 100 from the flip-flops (MSB first)). (CO4)
10. The 100 kHz square waveform of Fig. 2 (a) is applied to the clock input of the flip-flops shown in Figs. 2(b) and (c). If the Q output is initially '0', draw the Q output waveform in the two cases. Also, determine the frequency of the Q output in the two cases. (CO4)



(a)



(b)

(c)

Fig. 2